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XIO2200A PCI Express to PCI Bus Translation Bridge with 1394a OHCI and Two-Port PHY

Data Manual

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1 XIO2200A Features

- **Full x1 PCI Express Throughput**
- **Fully Compliant with *PCI Express to PCI/PCI-X Bridge Specification*, Revision 1.0**
- **Fully Compliant with *PCI Express Base Specification*, Revision 1.0a**
- **Fully Compliant with *PCI Local Bus Specification*, Revision 2.3**
- **A Second Virtual Channel for Quality-of-Service and Isochronous Applications**
- **Advanced PCI Isochronous Windows for Memory Space Mapping to a Specified Traffic Class**
- **Utilizes 100-MHz Differential PCI Express Common Reference Clock or 125-MHz Single-Ended Reference Clock**
- **Fully Compliant With Provisions of IEEE Std 1394-1995 for a High-Performance Serial Bus and IEEE Std 1394a-2000.**
- **Fully Compliant with *1394 Open Host Controller Interface Specification*, Revision 1.1**
- **Full IEEE Std 1394a–2000 Support Includes: Connection Debounce, Arbitrated Short Reset, Multispeed Concatenation, Arbitration Acceleration, Fly-by Concatenation, and Port Disable/Suspend/Resume**
- **Two IEEE Std 1394a-2000 Fully Compliant Cable Ports at 100M Bits/s, 200M Bits/s, and 400M Bits/s**
- **Cable Ports Monitor Line Conditions for Active Connection To Remote Node**
- **Cable Power Presence Monitoring**
- **EEPROM Configuration Support to Load the Global Unique ID for the 1394 Fabric**
- **Wake Event and Beacon Support**
- **Support for D1, D2, $D3_{hot}$, and $D3_{cold}$**
- **Active State Link Power Management Saves Power When Packet Activity on the PCI Express Link is Idle, Using Both L0s and L1 States**
- **Integrated AUX Power Switch Drains V_{AUX} Power Only When Main Power Is Off**
- **Eight 3.3-V, Multifunction, General-Purpose I/O Terminals**
- **Compact Footprint, 176-Ball, GGW MicroStar™ BGA, Lead-Free 176-Ball, ZGW MicroStar™ BGA, or Lead–Free 175–ball, ZHH MicroStar™ BGA**

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2 Introduction

The Texas Instruments XIO2200A is a single-function PCI Express to PCI local bus translation bridge where the PCI bus interface is internally connected to a 1394a-2000 open host controller link-layer controller with a two-port 1394a PHY. When the XIO2200A is properly configured, this solution provides full PCI Express and 1394a functionality and performance.

2.1 Description

The XIO2200A is a single-function PCI Express to PCI translation bridge where the PCI bus interface is internally connected to a 1394a open host controller link-layer controller with a two-port 1394a PHY. The PCI-Express to PCI translation bridge is fully compatible with the *PCI Express to PCI/PCI-X Bridge Specification*, Revision 1.0. Also, the bridge supports the standard PCI-to-PCI bridge programming model. The 1394a OHCI controller function is fully compatible with IEEE Standard 1394a-2000 and the latest 1394 *Open Host Controller Interface (OHCI) Specification*.

For downstream traffic, the PCI Express to PCI translation bridge simultaneously supports up to eight posted and four nonposted transactions for each enabled virtual channel (VC). For upstream traffic, up to six posted and four nonposted transactions are simultaneously supported for each VC.

The PCI Express interface supports a x1 link operating at full 250 MB/s packet throughput in each direction simultaneously. Two independent VCs are supported. The second VC is optimized for isochronous traffic types and quality-of-service (QoS) applications. Also, the bridge supports the advanced error reporting capability including ECRC as defined in the *PCI Express Base Specification*, Revision 1.0a. Supplemental firmware or software is required to fully utilize both of these features.

Robust pipeline architecture is implemented to minimize system latency across the bridge. If parity errors are detected, then packet poisoning is supported for both upstream and downstream operations.

Deep FIFOs are provided to buffer 1394 data and accommodate large host bus latencies. The bridge provides physical write posting and a highly tuned physical data path for SBP-2 performance. The bridge is capable of transferring data between the PCI Express bus and the 1394 bus at 100M bits/s, 200M bits/s, and 400M bits/s. The bridge provides two 1394 ports that have separate cable bias (TPBIAS). The bridge also supports the IEEE Std 1394a-2000 power-down features for battery-operated applications and arbitration enhancements.

As required by the *1394 Open Host Controller Interface Specification* and IEEE Std 1394a-2000, internal control registers are memory-mapped and nonprefetchable. This configuration header is accessed through configuration cycles specified by PCI Express, and it provides plug-and-play (PnP) compatibility.

The PHY-layer provides the digital and analog transceiver functions needed to implement a two-port node in a cable-based 1394 network. Each cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, for initialization and arbitration, and for packet reception and transmission. An external 2-wire serial EEPROM interface is provided to load the global unique ID for the 1394 fabric.

Power management (PM) features include active state link PM, PME mechanisms, the beacon and wake protocols, and all conventional PCI D-states. If the active state link PM is enabled, then the link automatically saves power when idle using the L0s and L1 states. PM active state NAK, PM PME, and PME-to-ACK messages are supported.

Eight general-purpose inputs and outputs (GPIOs), configured through accesses to the PCI Express configuration space, allow for further system control and customization.

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2.2 Related Documents

- *PCI Express to PCI/PCI-X Bridge Specification*, Revision 1.0
- *PCI Express Base Specification*, Revision 1.0a
- *PCI Express Card Electromechanical Specification*, Revision 1.0a
- *PCI Local Bus Specification*, Revision 2.3
- *PCI-to-PCI Bridge Architecture Specification*, Revision 1.2
- *PCI Bus Power Management Interface Specification*, Revision 1.1 or 1.2
- *1394 Open Host Controller Interface Specification* (Release 1.1)
- *IEEE Standard for a High Performance Serial Bus* (IEEE Std 1394-1995)
- *IEEE Standard for a High Performance Serial Bus—Amendment 1* (IEEE Std 1394a-2000)
- Express Card Standard, Release 1.0
- *PCI Express Jitter and BER White Paper*

2.3 Trademarks

- PCI Express is a trademark of PCI-SIG
- TI, OHCI-Lynx, and MicroStar BGA are trademarks of Texas Instruments Incorporated
- Other trademarks are the property of their respective owners

2.4 Document Conventions

Throughout this data manual, several conventions are used to convey information. These conventions are listed below:

1. To identify a binary number or field, a lower case b follows the numbers. For example: 000b is a 3-bit binary field.
2. To identify a hexadecimal number or field, a lower case h follows the numbers. For example: 8AFh is a 12-bit hexadecimal field.
3. All other numbers that appear in this document that do not have either a b or h following the number are assumed to be decimal format.
4. If the signal or terminal name has a bar above the name (for example, $\overline{\text{GRST}}$), then this indicates the logical NOT function. When asserted, this signal is a logic low, 0, or 0b.
5. Differential signal names end with P, N, +, or – designators. The P or + designators signify the positive signal associated with the differential pair. The N or – designators signify the negative signal associated with the differential pair.
6. RSVD indicates that the referenced item is reserved.
7. The power and ground signals in Figure 2–1 are not subscripted to aid in readability.
8. In Sections 4 through 6, the configuration space for the bridge is defined. For each register bit, the software access method is identified in an access column. The legend for this access column includes the following entries:

   r – read access by software

   u – updates by the bridge internal hardware

   w – write access by software

   c – clear an asserted bit with a write-back of 1b by software
9. The XIO2200A consists of a PCI-Express to PCI translation bridge where the secondary PCI bus is internally connected to a 1394a OHCI with a 2-port PHY. When describing functionality that is specific to the PCI-Express to PCI translation bridge, the term bridge is used to reduce text. The term 1394a OHCI is used to reduce text when describing the 1394a OHCI with 2-port PHY function.

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2.5 Document History

REVISION DATE	REVISION NUMBER	REVISION COMMENTS
08/2005	–	Initial release
01/2007	–	Add ZHH package information

2.6 Ordering Information

ORDERING NUMBER	NAME	VOLTAGE	PACKAGE
XIO2200A	PCI-Express to PCI Translation Bridge with 1394a OHCI and Two-Port PHY	3.3-V and 1.5-V power terminals	176-terminal GGW MicroStar BGA
XIO2200A	PCI-Express to PCI Translation Bridge with 1394a OHCI and Two-Port PHY	3.3-V and 1.5-V power terminals	176-terminal ZGW (Lead-Free) MicroStar BGA
XIO2200A	PCI-Express to PCI Translation Bridge with 1394a OHCI and Two-Port PHY	3.3-V and 1.5-V power terminals	175-terminal ZHH (Lead-Free) MicroStar BGA

2.7 Terminal Assignments

The XIO2200A is available in either a 176-ball GGW/ZGW MicroStar™ BGA or a 175–ball ZHH MicroStar™ BGA package.

Figure 2–1 is a terminal diagram of the GGW/ZGW package, and Table 2–1 lists the GGW/ZGW package terminals in alphanumerical order.

Figure 2–2 is a terminal diagram of the ZHH package, and Table 2–2 lists the ZHH package terminals in alphanumerical order.

Table 2–3 lists the terminals by the alphabetically sorted signal names for both packages.

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	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
U		RSVD	RSVD	RSVD	GPIO1	GPIO3	GPIO6	GPIO7	CNA	PC0	TPB0N	TPA0N	TPBIAS 0	TPB1N	TPA1N	TPBIAS 1	
T	RSVD		RSVD	RSVD	GPIO0	GPIO2	GPIO5 // SDA	RSVD	PC1	CPS	TPB0P	TPA0P	VDDA_ 33	TPB1P	TPA1P		R0_ 1394
R	RSVD	RSVD		VSS	VDD_33	VSS	GPIO4 // SCL	RSVD	PC2	VSSA	VSSA	VSSA	VSSA	VDDA_ 33		R1_ 1394	VSSA
P	RSVD	RSVD	RSVD				VDD_15	VSS	VDD_33	VDDA_ 33	VDDA_ 33				VDDA _15	XO	XI
N	RSVD	RSVD	VSS												RSVD	RSVD	$\overline{\text{GRST}}$
M	RSVD	RSVD	VDD_33												RSVD	$\overline{\text{WAKE}}$	VDD_15 _COMB
L	RSVD	RSVD	RSVD	RSVD										VDD_33 _COMB IO	VSSA	REF0_ PCIE	REF1_ PCIE
K	RSVD	RSVD	RSVD	VSS										VDD_33 _AUX	VDDA_ 33	VDD_33 _COMB	VSS
J	VDD_33	RSVD	RSVD	VDD_15										VDDA_ 15	VDDA_ 15	VSSA	$\overline{\text{PERST}}$
H	RSVD	RSVD	RSVD	VDD_33										VDD_15	VSSA	TXN	TXP
G	RSVD	RSVD	RSVD	VSS										VSSA	VDDA_ 15	VSSA	VSS
F	RSVD	RSVD	RSVD												VSSA	VSSA	VDDA_ 15
E	RSVD	RSVD	VDD_33												VSSA	RXN	RXP
D	RSVD	RSVD	VSS				RSVD	VSS	VDD_15	VDD_33	VSS				VDDA_ 33	RSVD	RSVD
C	RSVD	RSVD		RSVD	VSS	VDD_33	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	VDD_33	VSS		REF CLK–	REF CLK+
B	RSVD		RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD		VSSA
A		RSVD	RSVD	VDD_33	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	REFCLK _SEL	
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

Figure 2–1. XIO2200A GGW/ZGW MicroStar BGA™ Package (Bottom View)

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Table 2–1. XIO2200A GGW/ZGW Terminals Sorted Alphanumerically

BGA BALL #	SIGNAL NAME	BGA BALL #	SIGNAL NAME	BGA BALL #	SIGNAL NAME
A02	RSVD	C17	REFCLK+	J14	VDDA_15
A03	RSVD	D01	RSVD	J15	VDDA_15
A04	VDD_33	D02	RSVD	J16	VSSA
A05	RSVD	D03	VSS	J17	$\overline{\text{PERST}}$
A06	RSVD	D07	RSVD	K01	RSVD
A07	RSVD	D08	VSS	K02	RSVD
A08	RSVD	D09	VDD_15	K03	RSVD
A09	RSVD	D10	VDD_33	K04	VSS
A10	RSVD	D11	VSS	K14	VDD_33_AUX
A11	RSVD	D15	VDDA_33	K15	VDDA_33
A12	RSVD	D16	RSVD	K16	VDD_33_COMB
A13	RSVD	D17	RSVD	K17	VSS
A14	RSVD	E01	RSVD	L01	RSVD
A15	RSVD	E02	RSVD	L02	RSVD
A16	REFCLK_SEL	E03	VDD_33	L03	RSVD
B01	RSVD	E15	VSSA	L04	RSVD
B03	RSVD	E16	RXN	L14	VDD_33_COMBIO
B04	RSVD	E17	RXP	L15	VSSA
B05	RSVD	F01	RSVD	L16	REF0_PCIE
B06	RSVD	F02	RSVD	L17	REF1_PCIE
B07	RSVD	F03	RSVD	M01	RSVD
B08	RSVD	F15	VSSA	M02	RSVD
B09	RSVD	F16	VSSA	M03	VDD_33
B10	RSVD	F17	VDDA_15	M15	RSVD
B11	RSVD	G01	RSVD	M16	$\overline{\text{WAKE}}$
B12	RSVD	G02	RSVD	M17	VDD_15_COMB
B13	RSVD	G03	RSVD	N01	RSVD
B14	RSVD	G04	VSS	N02	RSVD
B15	RSVD	G14	VSSA	N03	VSS
B17	VSSA	G15	VDDA_15	N15	RSVD
C01	RSVD	G16	VSSA	N16	RSVD
C02	RSVD	G17	VSS	N17	$\overline{\text{GRST}}$
C04	RSVD	H01	RSVD	P01	RSVD
C05	VSS	H02	RSVD	P02	RSVD
C06	VDD_33	H03	RSVD	P03	RSVD
C07	RSVD	H04	VDD_33	P07	VDD_15
C08	RSVD	H14	VDD_15	P08	VSS
C09	RSVD	H15	VSSA	P09	VDD_33
C10	RSVD	H16	TXN	P10	VDDA_33
C11	RSVD	H17	TXP	P11	VDDA_33
C12	RSVD	J01	VDD_33	P15	VDDA_15
C13	VDD_33	J02	RSVD	P16	XO
C14	VSS	J03	RSVD	P17	XI
C16	REFCLK–	J04	VDD_15	R01	RSVD

Not Recommended for New Designs

Table 2–1. XIO2200A GGW/ZGW Terminals Sorted Alphanumerically (Continued)

BGA BALL #	SIGNAL NAME	BGA BALL #	SIGNAL NAME	BGA BALL #	SIGNAL NAME
R02	RSVD	T03	RSVD	U03	RSVD
R04	VSS	T04	RSVD	U04	RSVD
R05	VDD_33	T05	GPIO0	U05	GPIO1
R06	VSS	T06	GPIO2	U06	GPIO3
R07	GPIO4 // SCL	T07	GPIO5 // SDA	U07	GPIO6
R08	RSVD	T08	RSVD	U08	GPIO7
R09	PC2	T09	PC1	U09	CNA
R10	VSSA	T10	CPS	U10	PC0
R11	VSSA	T11	TPB0P	U11	TPB0N
R12	VSSA	T12	TPA0P	U12	TPA0N
R13	VSSA	T13	VDDA_33	U13	TPBIAS0
R14	VDDA_33	T14	TPB1P	U14	TPB1N
R16	R1_1394	T15	TPA1P	U15	TPA1N
R17	VSSA	T17	R0_1394	U16	TPBIAS1
T01	RSVD	U02	RSVD		

	01	02	03	04	05	06	07	08	09	10	11	12	13	14	
P	RSVD	RSVD	RSVD	GPIO0	GPIO4 //SCL	RSVD	PC2	TPB0P	TPA0P	TPB1P	TPA1P	TPBIAS1	VSSA	R0_1394	P
N	RSVD	RSVD	RSVD	GPIO2	GPIO5 //SDA	CNA	PC0	TPBoN	TPA0N	TPB1N	TPA1N	VDD_15	VSSA	R1_1394	N
M	RSVD	RSVD	RSVD	GPIO3	GPIO6	RSVD	PC1	VSSA	VDDA_ 33	VDDA_ 33	VDDA_ 33	RSVD	XO	XI	M
L	RSVD	RSVD	RSVD	RSVD	VDD_15	GPIO7	CPS	VDDA_ 33	VSSA	TPBIAS0	VSSA	RSVD	$\overline{\text{GRST}}$	RSVD	L
K	RSVD	RSVD	RSVD	VDD_33							VSSA	VDD_33 _COM-BIO	VDD_15 _COMB	$\overline{\text{WAKE}}$	K
J	RSVD	RSVD	RSVD	RSVD		VDD_33	VDD_33	VSS	VSS		VDDA_ 33	VDDA_ 33_AUX	REF1_ PCIE	REF0_ PCIE	J
H	RSVD	RSVD	RSVD	RSVD		VSS	VSS	VSS	VSS		VDDA_ 15	$\overline{\text{PERST}}$	VDDA_ 15	VDD_33 _COMB	H
G	VCCP	RSVD	RSVD	VDD_15		VSS	VSS	VSS	VSS		VSSA	VSSA	TXN	TXP	G
F	RSVD	RSVD	RSVD	VDD_33		VSS	VSS	VSS	VDD_33		VSSA	VDDA_ 15	VSS	VDD_15	F
E	RSVD	RSVD	RSVD	RSVD							VDDA_ 15	VSSA	RXN	RXP	E
D	RSVD	RSVD	RSVD	VDD_33	VDD_33	RSVD	RSVD	VDD_15	VDD_33	RSVD	RSVD	VSSA	RSVD	RSVD	D
C	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	VDDA_ 33	REF CLK+	REF CLK–	C
B	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	VSSA	B
A		RSVD	RSVD	VDD_33	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	REFCLK _SEL	A
	01	02	03	04	05	06	07	08	09	10	11	12	13	14	

Figure 2–2. XIO2200A ZHH MicroStar BGA™ Package (Bottom View)

Not Recommended for New Designs

Table 2–2. XIO2200A ZHH Terminals Sorted Alphanumerically

BGA BALL #	SIGNAL NAME	BGA BALL #	SIGNAL NAME	BGA BALL #	SIGNAL NAME
A02	RSVD	D04	VDD_33	H02	RSVD
A03	RSVD	D05	VDD_33	H03	RSVD
A04	VDD_33	D06	RSVD	H04	RSVD
A05	RSVD	D07	RSVD	H06	VSS
A06	RSVD	D08	VDD_15	H07	VSS
A07	RSVD	D09	VDD_33	H08	VSS
A08	RSVD	D10	RSVD	H09	VSS
A09	RSVD	D11	RSVD	H11	VDDA_15
A10	RSVD	D12	VSSA	H12	$\overline{\text{PERST}}$
A11	RSVD	D13	RSVD	H13	VDDA_15
A12	RSVD	D14	RSVD	H14	VDD_33_COMB
A13	RSVD	E01	RSVD	J01	RSVD
A14	REFCLK_SEL	E02	RSVD	J02	RSVD
B01	RSVD	E03	RSVD	J03	RSVD
B02	RSVD	E04	RSVD	J04	RSVD
B03	RSVD	E11	VSSA_15	J06	VDD_33
B04	RSVD	E12	VSSA	J07	VDD_33
B05	RSVD	E13	RXN	J08	VSS
B06	RSVD	E14	RXP	J09	VSS
B07	RSVD	F01	RSVD	J11	VDDA_33
B08	RSVD	F02	RSVD	J12	VDD_33_AUX
B09	RSVD	F03	RSVD	J13	REF1_PCIE
B10	RSVD	F04	VDD_33	J14	REF0_PCIE
B11	RSVD	F06	VSS	K01	RSVD
B12	RSVD	F07	VSS	K02	RSVD
B13	RSVD	F08	VSS	K03	RSVD
B14	VSSA	F09	VDD_33	K04	VDD_33
C01	RSVD	F11	VSSA	K11	VSSA
C02	RSVD	F12	VDDA_15	K12	VDD_33_COMBIO
C03	RSVD	F13	VSS	K13	VDD_15_COMB
C04	RSVD	F14	VDD_15	K14	$\overline{\text{WAKE}}$
C05	RSVD	G01	VDD_33	L01	RSVD
C06	RSVD	G02	RSVD	L02	RSVD
C07	RSVD	G03	RSVD	L03	RSVD
C08	RSVD	G04	VDD_15	L04	RSVD
C09	RSVD	G06	VSS	L05	VDD_15
C10	RSVD	G07	VSS	L06	GPIO7
C11	RSVD	G08	VSS	L07	CPS
C12	VDDA_33	G09	VSS	L08	VDDA_33
C13	REFCLK+	G11	VSSA	L09	VSSA
C14	REFCLK–	G12	VSSA	L10	TBPIAS0
D01	RSVD	G13	TXN	L11	VSSA
D02	RSVD	G14	TXP	L12	RSVD
D03	RSVD	H01	RSVD	L13	$\overline{\text{GRST}}$

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Table 2–2. XIO2200A ZHH Terminals Sorted Alphanumerically (Continued)

BGA BALL #	SIGNAL NAME	BGA BALL #	SIGNAL NAME	BGA BALL #	SIGNAL NAME
L14	RSVD	N01	RSVD	P02	RSVD
M01	RSVD	N02	RSVD	P03	GPIO0
M02	RSVD	N03	RSVD	P04	GPIO1
M03	RSVD	N04	GPIO2	P05	GPIO4 // SCL
M04	GPIO3	N05	GPIO5 // SDA	P06	RSVD
M05	GPIO6	N06	CNA	P07	PC2
M06	RSVD	N07	PC0	P08	TPB0P
M07	PC1	N08	TPB0N	P09	TPA0P
M08	VSSA	N09	TPA0N	P10	TPB1P
M09	VDDA_33	N10	TPB1N	P11	TPA1P
M10	VDDA_33	N11	TPA1N	P12	TPBIAS1
M11	VDDA_33	N12	VDDA_15	P13	VSSA
M12	RSVD	N13	VSSA	P14	R0_1394
M13	XO	N14	R1_1394		
M14	XI	P01	RSVD		

Not Recommended for New Designs

Table 2–3. XIO2200A Signal Names Sorted Alphabetically

SIGNAL NAME	GGW/ZGW BALL #	ZHH BALL #	SIGNAL NAME	GGW/ZGW BALL #	ZHH BALL #	SIGNAL NAME	GGW/ZGW BALL #	ZHH BALL #
CNA	U09	N06	RSVD	B09	C02	RSVD	M15	L12
CPS	T10	L07	RSVD	B10	C03	RSVD	N01	K03
GPIO0	T05	P03	RSVD	B11	A10	RSVD	N02	L01
GPIO1	U05	P04	RSVD	B12	A11	RSVD	N15	L02
GPIO2	T06	N04	RSVD	B13	A12	RSVD	N16	L04
GPIO3	U06	M04	RSVD	B14	C04	RSVD	P01	L14
GPIO4 // SCL	R07	P05	RSVD	B15	B13	RSVD	P02	M06
GPIO5 // SDA	T07	N05	RSVD	C01	C05	RSVD	P03	L03
GPIO6	U07	M05	RSVD	C02	C06	RSVD	R01	M01
GPIO7	U08	L06	RSVD	C04	C07	RSVD	R02	M02
$\overline{\text{GRST}}$	N17	L13	RSVD	C07	C10	RSVD	R08	M12
PC0	U10	N07	RSVD	C09	A08	RSVD	T01	N01
PC1	T09	M07	RSVD	C10	C09	RSVD	T03	M03
PC2	R09	P07	RSVD	C11	C11	RSVD	T04	N03
$\overline{\text{PERST}}$	J17	H12	RSVD	C12	D02	RSVD	T08	P01
R0_1394	T17	P14	RSVD	D01	D06	RSVD	U02	N02
R1_1394	R16	N14	RSVD	D02	D07	RSVD	U03	P02
REF0_PCIE	L16	J14	RSVD	D07	D10	RSVD	U04	P06
REF1_PCIE	L17	J13	RSVD	D16	D14	RXN	E16	E13
REFCLK_SEL	A16	A14	RSVD	D17	D13	RXP	E17	E14
REFCLK–	C16	C14	RSVD	E01	D01	TPA0N	U12	N09
REFCLK+	C17	C13	RSVD	E02	D11	TPA0P	T12	P09
RSVD	A02	A02	RSVD	F01	E02	TPA1N	U15	N11
RSVD	A03	A03	RSVD	F02	E03	TPA1P	T15	P11
RSVD	A05	A05	RSVD	F03	D03	TPB0N	U11	N08
RSVD	A06	A06	RSVD	G01	F01	TPB0P	T11	P08
RSVD	A07	A07	RSVD	G02	E04	TPB1N	U14	N10
RSVD	A08	A09	RSVD	G03	E01	TPB1P	T14	P10
RSVD	A09	A13	RSVD	H01	F02	TPBIAS0	U13	L10
RSVD	A10	B01	RSVD	H02	F03	TPBIAS1	U16	P12
RSVD	A11	B02	RSVD	H03	G02	TXN	H16	G13
RSVD	A12	B03	RSVD	J02	G03	TXP	H17	G14
RSVD	A13	B04	RSVD	J03	H01	VDD_15	D09	D08
RSVD	A14	B05	RSVD	K01	H02	VDD_15	H14	F14
RSVD	A15	B12	RSVD	K02	H03	VDD_15	J04	G04
RSVD	B01	B06	RSVD	K03	H04	VDD_15	P07	L05
RSVD	B03	B08	RSVD	L01	J01	VDD_15_COMB	M17	K13
RSVD	B04	B09	RSVD	L02	J02	VDD_33	A04	A04
RSVD	B05	B10	RSVD	L03	J03	VDD_33	C06	D04
RSVD	B06	B11	RSVD	L04	J04	VDD_33	C13	D05
RSVD	B07	C01	RSVD	M01	K01	VDD_33	D10	D09
RSVD	B08	B07	RSVD	M02	K02	VDD_33	E03	F04

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Table 2–3. XIO2200A Signal Names Sorted Alphabetically (Continued)

SIGNAL NAME	GGW/ZGW BALL #	ZHH BALL #	SIGNAL NAME	GGW/ZGW BALL #	ZHH BALL #	SIGNAL NAME	GGW/ZGW BALL #	ZHH BALL #
VDD_33	H04	F09	VDDA_33	R14	M10	VSSA	E15	D12
VDD_33	J01	G01	VDDA_33	T13	M11	VSSA	F15	E12
VDD_33	M03	J06	VSS	C05	F06	VSSA	F16	F11
VDD_33	P09	J07	VSS	C14	F07	VSSA	G14	G11
VDD_33	R05	K04	VSS	D03	F08	VSSA	G16	G12
VDD_33_AUX	K14	J12	VSS	D08	F13	VSSA	H15	K11
VDD_33_COMB	K16	H14	VSS	D11	G07	VSSA	J16	L09
VDD_33_COMBIO	L14	K12	VSS	G04	G08	VSSA	L15	L11
VDDA_15	F17	E11	VSS	G17	G09	VSSA	R10	M08
VDDA_15	G15	F12	VSS	K04	H06	VSSA	R11	N13
VDDA_15	J14	H11	VSS	K17	H07	VSSA	R12	P13
VDDA_15	J15	H13	VSS	N03	H08	VSSA	R13	
VDDA_15	P15	N12	VSS	P08	H09	VSSA	R17	
VDDA_33	D15	C12	VSS	R04	J08	$\overline{\text{WAKE}}$	M16	K14
VDDA_33	K15	J11	VSS	R06	J09	XI	P17	M14
VDDA_33	P10	L08	VSS		G06	XO	P16	M13
VDDA_33	P11	M09	VSSA	B17	B14			

Not Recommended for New Designs

2.8 Terminal Descriptions

Table 2–4 through Table 2–11 give a description of the terminals. These terminals are grouped in tables by functionality. Each table includes the terminal name, terminal number, I/O type, and terminal description.

The following list describes the different input/output cell types that appear in the terminal description tables:

- HS DIFF IN = High speed differential input
- HS DIFF OUT = High speed differential output
- LV CMOS = 3.3-V low voltage CMOS input or output with 3.3-V clamp rail
- BIAS = Input/output terminals that generate a bias voltage to determine a driver's operating current
- Feed through = these terminals connect directly to macros within the part and not through an input or output cell.
- PWR = Power terminal
- GND = Ground terminal

Table 2–4. Power Supply Terminals

SIGNAL	GGW/ZGW BALL #	ZHH BALL #	I/O TYPE	EXTERNAL PARTS	DESCRIPTION
VDD_15	D09, H14, J04, P07	D08, F14, G04, L05	PWR	Bypass capacitors	1.5-V digital core power terminals
VDD_33	A04, C06, C13, D10, E03, H04, J01, M03, P09, R05	A04, D04, D05, F04, F09, G01, J06, J07, K04	PWR	Bypass capacitors	3.3-V digital I/O power terminals
VDD_33_AUX	K14	J12	PWR	Bypass capacitors	3.3-V auxiliary power terminal **Note:** This terminal is connected to V_{SS} through a pulldown resistor if no auxiliary supply is present.
VDDA_15	F17, G15, J14, J15, P15	E11, F12, H11, H13, N12	PWR	Pi filter	1.5-V analog power terminal
VDDA_33	D15, K15, P10, P11, R14, T13	C12, J11, L08, M09, M10, M11	PWR	Pi filter	3.3-V analog power terminals

Table 2–5. Ground Terminals

SIGNAL	GGW/ZGW BALL #	ZHH BALL #	I/O TYPE	DESCRIPTION
VSS	C05, C14, D03, D08, D11, G04, G17, K04, K17, N03, P08, R04, R06	F06, F07, F08, F13, G06, G07, G08, G09, H06, H07, H08, H09, J08, J09	GND	Digital ground terminals
VSSA	B17, E15, F15, F16, G14, G16, H15, J16, L15, R10, R11, R12, R13, R17	B14, D12, E12, F11, G11, G12, K11, L09, L11, M08, N13, P13	GND	Analog ground terminals

Table 2–6. Combined Power Outputs

SIGNAL	GGW/ ZGW BALL #	ZHH BALL #	I/O TYPE	EXTERNAL PARTS	DESCRIPTION
VDD_15_COMB	M17	K13	Feed through	Bypass capacitors	Internally-combined 1.5-V main and V_{AUX} power output for external bypass capacitor filtering. Supplies all internal 1.5-V circuitry powered by V_{AUX}. **Caution:** Do not use this terminal to supply external power.
VDD_33_COMB	K16	H14	Feed through	Bypass capacitors	Internally-combined 3.3-V main and V_{AUX} power output for external bypass capacitor filtering. Supplies all internal 3.3-V circuitry powered by V_{AUX}. **Caution:** Do not use this terminal to supply external power.
VDD_33_COMBIO	L14	K12	Feed through	Bypass capacitors	Internally-combined 3.3-V main and V_{AUX} power output for external bypass capacitor filtering. Supplies all internal 3.3-V input/output circuitry powered by V_{AUX}. **Caution:** Do not use this terminal to supply external power.

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Table 2–7. PCI Express Terminals

SIGNAL	GGW/ ZGW BALL #	ZHH BALL #	I/O TYPE	CELL TYPE	CLAMP RAIL	EXTERNAL PARTS	DESCRIPTION
$\overline{\text{PERST}}$	J17	H12	I	LV CMOS	VDD_33_ COMBIO	–	PCI Express reset input. The $\overline{\text{PERST}}$ signal identifies when the system power is stable and generates an internal power-on reset. **Note:** The $\overline{\text{PERST}}$ input buffer has hysteresis.
REF0_PCIE REF1_PCIE	L16 L17	J14 J13	I/O	BIAS	–	External resistor	External reference resistor + and – terminals for setting TX driver current. An external resistor is connected between terminals L16 and L17.
RXP RXN	E17 E16	E14 E13	DI	HS DIFF IN	VDD_15	–	High-speed receive pair. RXP and RXN comprise the differential receive pair for the single PCI Express lane supported.
TXP TXN	H17 H16	G14 G13	DO	HS DIFF OUT	VSS	Series capacitors	High-speed transmit pair. TXP and TXN comprise the differential transmit pair for the single PCI Express lane supported.
$\overline{\text{WAKE}}$	M16	K14	O	LV CMOS	VDD_33_ COMBIO	–	Wake is an active low signal that is driven low to reactivate the PCI Express link hierarchy's main power rails and reference clocks. **Note:** Since $\overline{\text{WAKE}}$ is an open-drain output buffer, a system side pullup resistor is required.

Table 2–8. Clock Terminals

SIGNAL	GGW/ ZGW BALL #	ZHH BALL #	I/O TYPE	CELL TYPE	CLAMP RAIL	EXTERNAL PARTS	DESCRIPTION
REFCLK_SEL	A16	A14	I	LV CMOS	VDD_33	Pullup or pulldown resistor	Reference clock select. This terminal selects the reference clock input. 0 = 100-MHz differential common reference clock used 1 = 125-MHz single-ended reference clock used
REFCLK+	C17	C13	DI	HS DIFF IN	VDD_33	–	Reference clock. REFCLK+ and REFCLK– comprise the differential input pair for the 100-MHz system reference clock. For a single-ended, 125-MHz system reference clock, use the REFCLK+ input.
REFCLK–	C16	C14	DI	HS DIFF IN	VDD_33	Capacitor to VSS for single-ended mode	Reference clock. REFCLK+ and REFCLK– comprise the differential input pair for the 100-MHz system reference clock. For a single-ended, 125-MHz system reference clock, attach a capacitor from REFCLK– to VSS.

Not Recommended for New Designs

Table 2–9. 1394 Terminals

SIGNAL	GGW/ ZGW BALL #	ZHH BALL #	I/O TYPE	CELL TYPE	EXTERNAL PARTS	DESCRIPTION
CNA	U09	N06	I/O	LV CMOS	–	Cable not active. This terminal is asserted high when there are no ports receiving incoming bias voltage. If it is not used, then this terminal must be strapped to GND through a resistor.
CPS	T10	L07	I	Feed through	External resistor per 1394a specification	Cable power status input. This terminal is normally connected to cable power through a 400-kΩ resistor. This circuit drives an internal comparator that detects the presence of cable power. If CPS is not used to detect cable power, then this terminal must be connected to VSSA.
PC0 PC1 PC2	U10 T09 R09	N07 M07 P07	I	LV CMOS	External resistor per 1394a specification	Power class programming inputs. On hardware reset, these inputs set the default value of the power class indicated during self-ID. Programming is done by tying these terminals high or low.
R0_1394 R1_1394	T17 R16	P14 N14	I/O	Bias	External resistor per 1394a specification	Current-setting resistor terminals. These terminals are connected to an external resistance to set the internal operating currents and cable driver output currents. A resistance of 6.34 kΩ ±1% is required to meet the IEEE Std 1394-1995 output voltage limits.
TPA0P TPA0N	T12 U12	P09 N09	I/O	LV CMOS	External resistors and capacitors per 1394a specification	Twisted-pair cable A differential signal terminals. Board trace lengths from each pair of positive and negative differential signal pins must be matched and as short as possible to the external load resistors and to the cable connector. For an unused port, TPA+ and TPA– can be left open.
TPA1P TPA1N	T15 U15	P11 N11	I/O	LV CMOS		
TPBIAS0 TPBIAS1	U13 U16	L10 P12	O	Bias	External resistors and capacitors per 1394a specification	Twisted-pair bias output. This provides the 1.86-V nominal bias voltage needed for proper operation of the twisted-pair cable drivers and receivers and for signaling to the remote nodes that there is an active cable connection. Each of these pins must be decoupled with a 1.0-µF capacitor to ground.
TPB0P TPB0N	T11 U11	P08 N08	I/O	LV CMOS	External resistors and capacitors per 1394a specification	Twisted-pair cable B differential signal terminals. Board trace lengths from each pair of positive and negative differential signal pins must be matched and as short as possible to the external load resistors and to the cable connector. For an unused port, TPB+ and TPB– can be left open.
TPB1P TPB1N	T14 U14	P10 N10	I/O	LV CMOS		
XI XO	P17 P16	M14 M13	I	Feed through	Crystal oscillator per 1394a specification	Crystal oscillator inputs. These terminals connect to a 24.576-MHz parallel resonant fundamental mode crystal. When an external clock source is used, XI must be the input and XO must be left open. The clock must be supplied before the device is taken out of reset.

Table 2–10. Reserved Terminals

SIGNAL	GGW/ZGW BALL #	ZHH BALL #	I/O TYPE	DESCRIPTION
RSVD	A02, A03, A05, A06, A07, A08, A09, A10, A11, A12, A13, A14, B01, B03, B04, B05, B06, B07, B09, B10, B14, C01, C02, C04, C07, C08, C11, C12, D01, D02, D07, E02, H01, H02, H03, J02, J03, K01, K02, K03, L01, L02, L03, L04, M01, M02, N01, N02, N15, N16, P01, P02, R08, T08, U03, U04	A02, A03, A05, A06, A07, A09, A13, B01, B02, B03, B04, B05, B06, B08, B09, B10, B11, C01, C02, C03, C04, C05, C06, C07, C08, C09, C10, C11, D02, D06, D07, D10, D11, F02, F03, G02, G03, H01, H02, H03, H04, J01, J02, J03, J04, K01, K02, K03, L01, L02, L04, L14, M06, M12, P01, P02, P06	O	Reserved, do not connect to external signals.

Not Recommended for New Designs

RSVD	B08, B11, B12, B13, C09, C10, E01, F01, F02, F03, G01, G02, G03, R01, R02, T01, T03, U02	A08, A10, A11, A12, B07, C09, D01, D03, E01, E02, E03, E04, F01, M01, M02, M03, N01, N02	I	Must be connected to VDD_33.
RSVD	A15, B15, D16, D17, P03, T04	B12, B13, D13, D14, L03, N03	I	Must be connected to VSS.
RSVD	M15	L12	I	If the V_{AUX} supply is present, connect this terminal to VDD_33_AUX. If the V_{AUX} supply is not present, connect this terminal to VDD_33.

Not Recommended for New Designs

Table 2–11. Miscellaneous Terminals

SIGNAL	GGW/ ZGW BALL #	ZHH BALL #	I/O TYPE	CELL TYPE	CLAMP RAIL	EXTERNAL PARTS	DESCRIPTION
GPIO0	T05	P03	I/O	LV CMOS	VDD_33	–	General-purpose I/O 0. This terminal functions as a GPIO controlled by bit 0 (GPIO0_DIR) in the GPIO control register (see Section 4.59). **Note:** This terminal has an internal active pullup resistor.
GPIO1	U05	P04	I/O	LV CMOS	VDD_33	–	General-purpose I/O 1. This terminal functions as a GPIO controlled by bit 1 (GPIO1_DIR) in the GPIO control register (see Section 4.59). **Note:** This terminal has an internal active pullup resistor.
GPIO2	T06	N04	I/O	LV CMOS	VDD_33	–	General-purpose I/O 2. This terminal functions as a GPIO controlled by bit 2 (GPIO2_DIR) in the GPIO control register (see Section 4.59). **Note:** When $\overline{\text{PERST}}$ is deasserted, this terminal must be a 1b to enable the PCI Express 1.0a compatibility mode. **Note:** This terminal has an internal active pullup resistor.
GPIO3	U06	M04	I/O	LV CMOS	V_{DD_33}	–	General-purpose I/O 3. This terminal functions as a GPIO controlled by bit 3 (GPIO3_DIR) in the GPIO control register (see Section 4.59). **Note:** This terminal has an internal active pullup resistor.
GPIO4 // SCL	R07	P05	I/O	LV CMOS	VDD_33	Optional pullup resistor	GPIO4 or serial-bus clock. This terminal functions as serial-bus clock if a pullup resistor is detected on SDA. If a pulldown resistor is detected on SDA, then this terminal functions as GPIO4. **Note:** In serial-bus mode, an external pullup resistor is required to prevent the SCL signal from floating. **Note:** This terminal has an internal active pullup resistor.
GPIO5 // SDA	T07	N05	I/O	LV CMOS	VDD_33	Pullup or pulldown resistor	GPIO5 or serial-bus data. This terminal functions as serial-bus data if a pullup resistor is detected on SDA. If a pulldown resistor is detected on SDA, then this terminal functions as GPIO5. **Note:** In serial-bus mode, an external pullup resistor is required to prevent the SDA signal from floating.
GPIO6	U07	M05	I/O	LV CMOS	VDD_33	–	General-purpose I/O 6. This terminal functions as a GPIO controlled by bit 6 (GPIO6_DIR) in the GPIO control register (see Section 4.59). **Note:** This terminal has an internal active pullup resistor.
GPIO7	U08	L06	I/O	LV CMOS	VDD_33	–	General-purpose I/O 7. This terminal functions as a GPIO controlled by bit 7 (GPIO7_DIR) in the GPIO control register (see Section 4.59). **Note:** This terminal has an internal active pullup resistor.
$\overline{\text{GRST}}$	N17	L13	I	LV CMOS	VDD_33_ COMBIO	–	Global reset input. Asynchronously resets all logic in device, including sticky bits and power management state machines. **Note:** The $\overline{\text{GRST}}$ input buffer has both hysteresis and an internal active pullup.

Not Recommended for New Designs

3 Feature/Protocol Descriptions

This chapter provides a high-level overview of all significant device features. Figure 3–1 shows a simplified block diagram of the basic architecture of the PCI-Express to PCI Bridge with 1394a OHCI and two-port PHY. The top of the diagram is the PCI Express interface and the 1394a OHCI with two-port PHY is located at the bottom of the diagram.

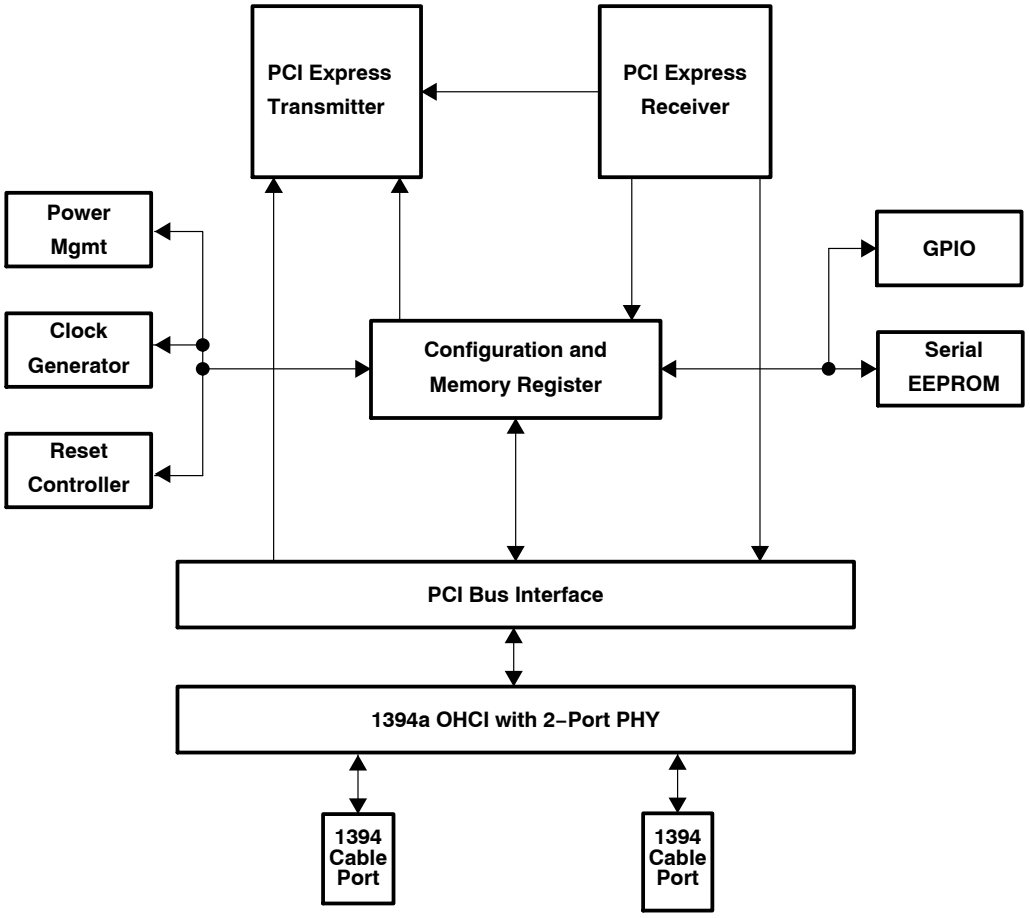

Figure 3–1. XIO2200A Block Diagram

3.1 Power-Up/-Down Sequencing

The bridge contains both 1.5-V and 3.3-V power terminals. In addition, a V_{AUX} supply exists to support the $D3_{cold}$ state. The following power-up and power-down sequences describe how power is applied to these terminals.

In addition, the bridge has three resets: $\overline{PERST}$, $\overline{GRST}$, and an internal power-on reset. These resets are fully described in Section 3.2. The following power-up and power-down sequences describe how $\overline{PERST}$ is applied to the bridge.

The application of the PCI Express reference clock (REFCLK) is important to the power-up/-down sequence and is included in the following power-up and power-down descriptions.

Not Recommended for New Designs

3.1.1 Power-Up Sequence

1. Assert $\overline{\text{PERST}}$ to the device.
2. Apply 1.5-V and 3.3-V voltages.
3. Apply a stable PCI Express reference clock.
4. To meet PCI Express specification requirements, $\overline{\text{PERST}}$ cannot be deasserted until the following two delay requirements are satisfied:
   - Wait a minimum of 100 µs after applying a stable PCI Express reference clock. The 100-µs limit satisfies the requirement for stable device clocks by the deassertion of $\overline{\text{PERST}}$.
   - Wait a minimum of 100 ms after applying power. The 100-ms limit satisfies the requirement for stable power by the deassertion of $\overline{\text{PERST}}$.

See the power-up sequencing diagram in Figure 3–2.

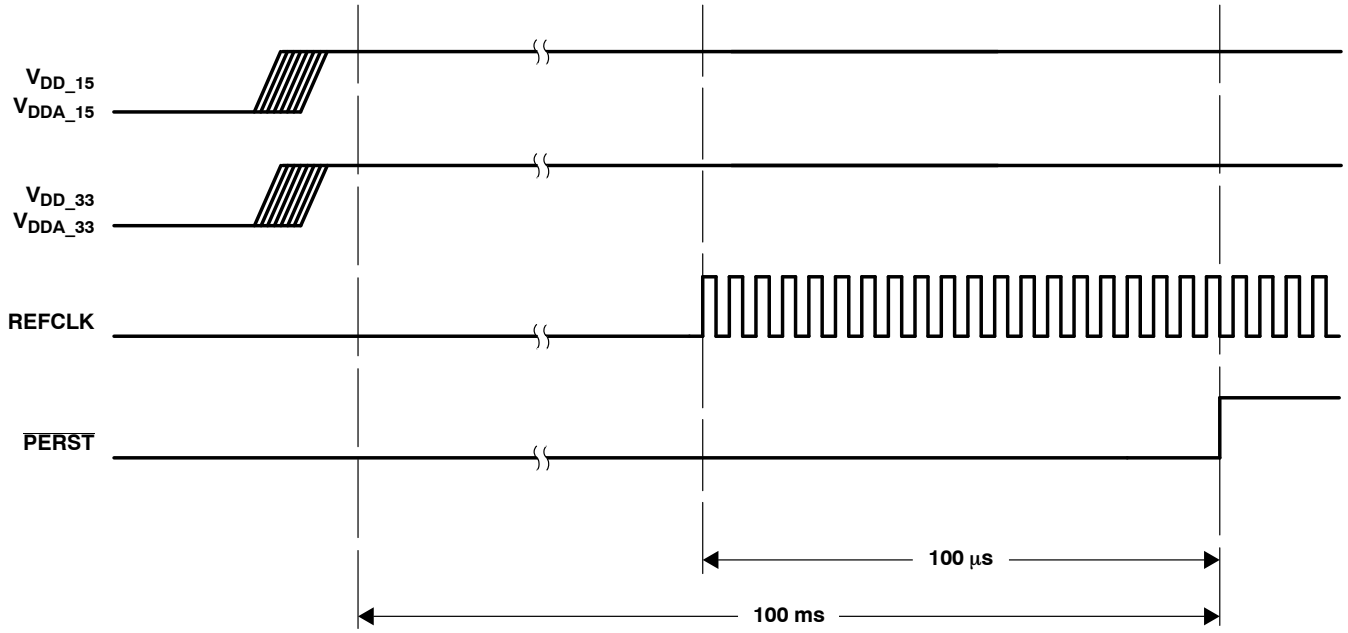

Figure 3–2. Power-Up Sequence

Not Recommended for New Designs

3.1.2 Power-Down Sequence

1. Assert $\overline{\text{PERST}}$ to the device.
2. Remove the reference clock.
3. Remove 3.3-V and 1.5-V voltages.

Please see the power-down sequencing diagram in Figure 3–3. If the VDD_33_AUX terminal is to remain powered after a system shutdown, then the bridge power-down sequence is exactly the same as shown in Figure 3–3.

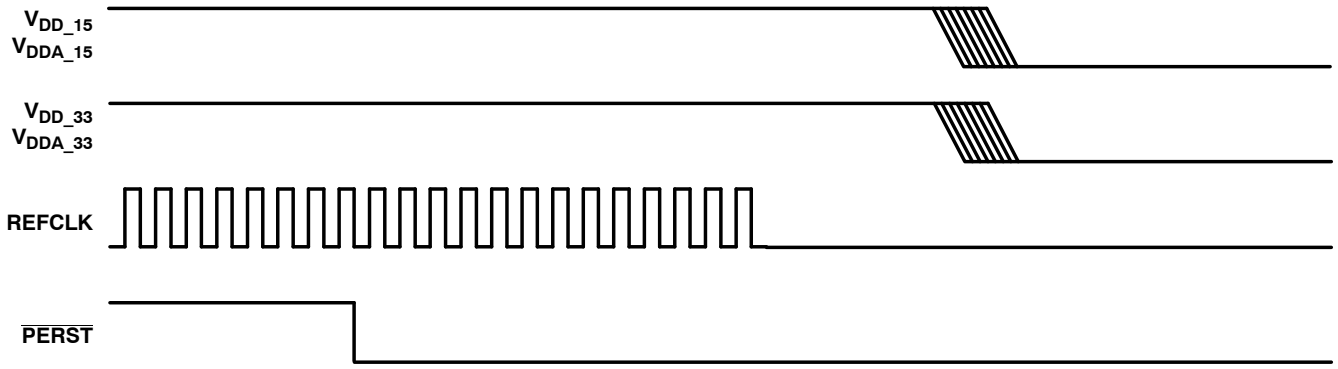

Figure 3–3. Power-Down Sequence

3.2 Bridge Reset Features

There are five bridge reset options that include internally-generated power-on reset, resets generated by asserting input terminals, and software-initiated resets that are controlled by sending a PCI Express hot reset or setting a configuration register bit. Table 3–1 identifies these reset sources and describes how the bridge responds to each reset.

Not Recommended for New Designs

Table 3–1. Bridge Reset Options

RESET OPTION	XIO2200A FEATURE	RESET RESPONSE
Bridge internally-generated power-on reset	During a power-on cycle, the bridge asserts an internal reset and monitors the VDD_15_COMB (M17) terminal. When this terminal reaches 90% of the nominal input voltage specification, power is considered stable. After stable power, the bridge monitors the PCI Express reference clock (REFCLK) and waits 10 µs after active clocks are detected. Then, internal power-on reset is deasserted.	When the internal power-on reset is asserted, all control registers, state machines, sticky register bits, and power management state machines are initialized to their default state. In addition, the bridge asserts the internal PCI bus reset.
Global reset input $\overline{\text{GRST}}$ (N17)	When $\overline{\text{GRST}}$ is asserted low, an internal power-on reset occurs. This reset is asynchronous and functions during both normal power states and V_{AUX} power states.	When $\overline{\text{GRST}}$ is asserted low, all control registers, state machines, sticky register bits, and power management state machines are initialized to their default state. In addition, the bridge asserts the internal PCI bus reset. When the rising edge of $\overline{\text{GRST}}$ occurs, the bridge samples the state of all static control inputs and latches the information internally. If an external serial EEPROM is detected, then a download cycle is initiated. Also, the process to configure and initialize the PCI Express link is started. The bridge starts link training within 80 ms after $\overline{\text{GRST}}$ is deasserted.
PCI Express reset input $\overline{\text{PERST}}$ (J17)	This bridge input terminal is used by an upstream PCI Express device to generate a PCI Express reset and to signal a system power good condition. When $\overline{\text{PERST}}$ is asserted low, the bridge generates an internal PCI Express reset as defined in the PCI Express specification. When $\overline{\text{PERST}}$ transitions from low to high, a system power good condition is assumed by the bridge. **Note:** The system must assert $\overline{\text{PERST}}$ before power is removed, before REFCLK is removed or before REFCLK becomes unstable.	When $\overline{\text{PERST}}$ is asserted low, all control register bits that are not sticky are reset. Within the configuration register maps, the sticky bits are indicated by the ☆ symbol. Also, all state machines that are not associated with sticky functionality or V_{AUX} power management are reset. In addition, the bridge asserts the internal PCI bus reset. When the rising edge of $\overline{\text{PERST}}$ occurs, the bridge samples the state of all static control inputs and latches the information internally. If an external serial EEPROM is detected, then a download cycle is initiated. Also, the process to configure and initialize the PCI Express link is started. The bridge starts link training within 80 ms after $\overline{\text{PERST}}$ is deasserted.
PCI Express training control hot reset	The bridge responds to a training control hot reset received on the PCI Express interface. After a training control hot reset, the PCI Express interface enters the DL_DOWN state.	In the DL_DOWN state, all remaining configuration register bits and state machines are reset. All remaining bits exclude sticky bits and EEPROM loadable bits. All remaining state machines exclude sticky functionality, EEPROM functionality, and V_{AUX} power management. Within the configuration register maps, the sticky bits are indicated by the ☆ symbol and the EEPROM loadable bits are indicated by the † symbol. In addition, the bridge asserts the internal PCI bus reset.
PCI bus reset	System software has the ability to assert and deassert the PCI bus reset on the secondary PCI bus interface.	When bit 6 (SRST) in the bridge control register at offset 3Eh (see Section 4.29) is asserted, the bridge asserts the internal PCI bus reset. A 0b in the SRST bit deasserts the PCI bus reset.

3.3 PCI Express Interface

3.3.1 External Reference Clock

The bridge requires either a differential, 100-MHz common clock reference or a single-ended, 125-MHz clock reference. The selected clock reference must meet all *PCI Express Electrical Specification* requirements for frequency tolerance, spread spectrum clocking, and signal electrical characteristics.

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If the REFCLK_SEL (A16) input is connected to V_{SS}, then a differential, 100-MHz common clock reference is expected by the bridge. If the A16 terminal is connected to V_{DD_33}, then a single-ended, 125-MHz clock reference is expected by the bridge.

When the single-ended, 125-MHz clock reference option is enabled, the single-ended clock signal is connected to the REFCLK+ (C17) terminal. The REFCLK− (C16) terminal is connected to one side of an external capacitor with the other side of the capacitor connected to V_{SS}.

When using a single-ended reference clock, care must be taken to ensure interoperability from a system jitter standpoint. The *PCI Express Base Specification* does not ensure interoperability when using a differential reference clock commonly used in PC applications along with a single-ended clock in a noncommon clock architecture. System jitter budgets will have to be verified to ensure interoperability. See the *PCI Express Jitter and BER White Paper* from the PCI-SIG.

3.3.2 Beacon

The bridge supports the PCI Express in-band beacon feature. Beacon is driven on the upstream PCI Express link by the bridge to request the reapplication of main power when in the L2 link state. To enable the beacon feature, bit 10 (BEACON_ENABLE) in the general control register at offset D4h is asserted. See Section 4.65, *General Control Register*, for details.

If the bridge is in the L2 link state and beacon is enabled, when a secondary PCI bus device asserts $\overline{\text{PME}}$, then the bridge outputs the beacon signal on the upstream PCI Express link. The beacon signal frequency is approximately 500 kHz ± 50% with a differential peak-to-peak amplitude of 500 mV and no de-emphasis. Once the beacon is activated, the bridge continues to send the beacon signal until main power is restored as indicated by $\overline{\text{PERST}}$ going inactive. At this time, the beacon signal is deactivated.

3.3.3 Wake

The bridge supports the PCI Express sideband $\overline{\text{WAKE}}$ feature. $\overline{\text{WAKE}}$ is an active low signal driven by the bridge to request the reapplication of main power when in the L2 link state. Since $\overline{\text{WAKE}}$ is an open-collector output, a system-side pullup resistor is required to prevent the signal from floating.

When the bridge is in the L2 link state and $\overline{\text{PME}}$ is received from a device on the secondary PCI bus, the $\overline{\text{WAKE}}$ signal is asserted low as a wakeup mechanism. Once $\overline{\text{WAKE}}$ is asserted, the bridge drives the signal low until main power is restored as indicated by $\overline{\text{PERST}}$ going inactive. At this time, $\overline{\text{WAKE}}$ is deasserted.

3.3.4 Initial Flow Control Credits

The bridge flow control credits are initialized using the rules defined in the *PCI Express Base Specification*. Table 3−2 identifies the initial flow control credit advertisement for the bridge. The initial advertisement is exactly the same when a second virtual channel (VC) is enabled.

Table 3−2. Initial Flow Control Credit Advertisements

CREDIT TYPE	INITIAL ADVERTISEMENT
Posted request headers (PH)	8
Posted request data (PD)	128
Nonposted header (NPH)	4
Nonposted data (NPD)	4
Completion header (CPLH)	0 (infinite)
Completion data (CPLD)	0 (infinite)

3.3.5 PCI Express Message Transactions

PCI Express messages are both initiated and received by the bridge. Table 3−3 outlines message support within the bridge.

Not Recommended for New Designs

Table 3–3. Messages Supported by the Bridge

MESSAGE	SUPPORTED	BRIDGE ACTION
Assert_INTx	Yes	Transmitted upstream
Deassert_INTx	Yes	Transmitted upstream
PM_Active_State_Nak	Yes	Received and processed
PM_PME	Yes	Transmitted upstream
PME_Turn_Off	Yes	Received and processed
PME_TO_Ack	Yes	Transmitted upstream
ERR_COR	Yes	Transmitted upstream
ERR_NONFATAL	Yes	Transmitted upstream
ERR_FATAL	Yes	Transmitted upstream
Set_Slot_Power_Limit	Yes	Received and processed
Unlock	No	Discarded
Hot plug messages	No	Discarded
Advanced switching messages	No	Discarded
Vendor defined type 0	No	Unsupported request
Vendor defined type 1	No	Discarded

All supported message transactions are processed per the *PCI Express Base Specification*.

3.4 Quality of Service and Isochronous Features

The bridge has both standard and advanced features that provide a robust solution for quality-of-service (QoS) and isochronous applications. These features are best described by divided them into the following three categories:

- PCI port arbitration. PCI port arbitration determines which bus master is granted the next transaction cycle on the PCI bus. The three PCI port arbitration options are the classic PCI arbiter, the 128-phase, weighted round-robin (WRR) time-based arbiter, and the 128-phase, WRR aggressive time-based arbiter. The power-up register default is the classic PCI arbiter. The advanced time-based arbiter features are provided to support isochronous applications.
- PCI isochronous windows. There are four separate windows that allow PCI bus-initiated memory transactions to be labeled with a PCI Express traffic class (TC) beyond the default TC0. Each window designates a range of PCI memory space that is mapped to a specified TC label. The power-up register default is all four windows disabled.
- PCI Express extended VC with VC arbitration. With an extended VC, system software can map a particular TC to a specific VC. The differentiated traffic on the second VC then uses dedicated system resources to support a QoS environment. VC arbitration is provided to gate traffic to the upstream PCI Express link. The three VC arbitration options include strict priority, hardware-fixed round-robin, and 32-phase WRR. The power-up register default is strict priority with the second VC disabled.

When configuring these standard and advanced features, the following rules must be followed:

1. The default mode is classic PCI arbiter with the PCI isochronous windows disabled and the second VC disabled. The bridge performs default PCI bus arbitration without any arbiter-related configuration register setup.
2. If a second VC is enabled, then at least one PCI isochronous window must be configured to map upstream transactions to the second VC.
3. If a second VC is enabled, then any VC arbiter option interacts with any PCI port arbiter option.
4. To enable the PCI isochronous windows it is not required to enable a second VC. The memory space to traffic mapping always uses VC0 for all upstream traffic.

5. When programming the upstream isochronous window base and limit registers, the 32-bit base/limit address must be DWORD aligned and the limit address must be greater than the base address.

The following sections describe in detail the standard and advanced bridge features for QoS and isochronous applications.

3.4.1 PCI Port Arbitration

The internal PCI port arbitration logic supports the internal 1394a OHCI and the bridge PCI bus devices. Three options exist when configuring the bridge arbiter: classic PCI arbiter, 128-phase, WRR time-based arbiter, and 128-phase, WRR aggressive time-based arbiter.

3.4.1.1 Classic PCI Arbiter

The classic PCI arbiter is configured through the classic PCI configuration space at offset DCh. Table 3–4 identifies and describes the registers associated with classic PCI arbitration mode.

Table 3–4. Classic PCI Arbiter Registers

PCI OFFSET	REGISTER NAME	DESCRIPTION
Classic PCI configuration register DCh	Arbiter control (see Section 4.69)	Contains a two-tier priority scheme for the bridge and 1394a OHCI functions. The bridge defaults to the high priority tier. The 1394a OHCI function defaults to the low priority tier. A bus parking control bit (bit 7, PARK) is provided.
Classic PCI configuration register DDh	Arbiter request mask (see Section 4.70)	Bit 0 (OHCI_MASK) provides individual control to block the 1394a OHCI $\overline{\text{REQ}}$ input. Bit 7 (ARB_TIMEOUT) enables the generating timeout status if the 1394a OHCI device does not respond within 16 PCI bus clocks. Bit 6 (AUTO_MASK) automatically masks a PCI bus $\overline{\text{REQ}}$ if the device does not respond after $\overline{\text{GNT}}$ is issued. The AUTO_MASK bit is cleared to disable any automatically generated mask.
Classic PCI configuration register DEh	Arbiter time-out status (see Section 4.71)	When bit 7 (ARB_TIMEOUT) in the arbiter request mask register (see Section 4.70) is asserted, timeout status for the 1394a OHCI device is reported in this register.

3.4.1.2 128-Phase, WRR Time-Based Arbiter

The 128-phase, WRR time-based arbiter is configured through the PCI express VC extended configuration space at offset 150h and the device control memory window register map.

The 128-phase, WRR time-based arbiter periodically asserts $\overline{\text{GNT}}$ to a PCI master device based on entries within a port arbitration table. There are actually two port arbitration tables within the bridge. The first table is accessed through the PCI Express VC extended configuration register space using configuration read/write transactions. The second table is internal and is used by the PCI bus arbiter to make $\overline{\text{GNT}}$ decisions. A configuration register load function exists to transfer the contents of the configuration register table to the internal table.

The port arbitration table uses a 4-bit field to identify the secondary bus master that receives $\overline{\text{GNT}}$ during each phase of the time-based WRR arbitration. For the arbiter to recognize a bus master $\overline{\text{REQ}}$ and to generate $\overline{\text{GNT}}$, software must allocate at least three consecutive phases to the same port number.

Table 3–5 defines the mapping relationship of the PCI bus devices to a port number in the port arbitration table.

Table 3–5. Port Number to PCI Bus Device Mapping

PORT NUMBER	$\overline{\text{GNT}}$	PCI DEVICE
0000b	Internal $\overline{\text{GNT}}$ for the bridge	Internal $\overline{\text{REQ}}$ from the bridge
0001b	Internal $\overline{\text{GNT}}$ for 1394a OHCI	Internal $\overline{\text{REQ}}$ from 1394a OHCI
0010b–1111b	Reserved	–

To enable the 128-phase, WRR time-based arbiter, two configuration registers must be written. Bit 1 (PORTARB_LEVEL_1_EN) in the upstream isochrony control register at offset 04h (see Section 6.4) within the device control memory window register map must be asserted. The VC1 resource control register at offset 170h within the PCI Express VC extended configuration space has a PORT_ARB_SELECT field that must be set to 100b (see Section 5.22).

Not Recommended for New Designs

Table 3–6 identifies and describes the registers associated with 128-phase, WWR time-based arbitration mode.

Table 3–6. 128-Phase, WRR Time-Based Arbiter Registers

REGISTER OFFSET	REGISTER NAME	DESCRIPTION
PCI Express VC extended configuration registers 1C0h to 1FCh	Port arbitration table (see Section 5.28)	16-doubleword sized configuration registers that are the registered version of the 128-phase, WRR port arbitration table. Each port arbitration table entry is a 4-bit field.
PCI Express VC extended configuration register 170h	VC1 resource control (see Section 5.25)	Bits 19:17 (PORT_ARB_SELECT) equal to 100b define the port arbitration mechanism as 128-phase WRR. Bit 16 (LOAD_PORT_TABLE), when written with a 1b, transfers the port arbitration table configuration register values to the internal registers used by the PCI bus arbiter.
PCI Express VC extended configuration register 176h	VC1 resource status (see Section 5.26)	Bit 0 (PORT_TABLE_STATUS) equal to 1b indicates that the port arbitration table configuration registers were updated but not loaded into the internal arbitration table.
Device control memory window register 04h	Upstream isochrony control (see Section 6.4)	Bit 1 (PORTARB_LEVEL_1_EN) must be asserted to enable the 128-phase, WRR time-based arbiter.

3.4.1.3 128-Phase, WRR Aggressive Time-Based Arbiter

The last option for PCI port arbitration is 128-phase, WRR aggressive time-based arbitration mode. This arbitration mode performs the same as isochronous mode arbitration, but with one difference. When an isochronous timing event occurs, the PCI bus arbiter deliberately stops a secondary bus master in the middle of the transaction to assure that isochrony is preserved. The register setup for this arbitration option is the same as the 128-phase, WRR time-based arbiter option with the following addition. Bit 2 (PORTARB_LEVEL_2_EN) in the device control memory window upstream isochrony control register at offset 04h must be asserted (see Section 6.4).

3.4.2 PCI Isochronous Windows

The bridge has four separate windows that allow PCI bus-initiated memory transactions to be labeled with a PCI Express traffic class (TC) beyond the default TC0. Each window designates a range of PCI memory space that is mapped to a specified TC label. This advance feature is configured through the device control memory window register map.

Table 3–7 identifies and describes the registers associated with isochronous arbitration mode.

Table 3–7. PCI Isochronous Windows

REGISTER OFFSET	REGISTER NAME	DESCRIPTION
Device control memory window register 08h	Upstream isochronous window 0 control (see Section 6.5)	Bit 0 (ISOC_WINDOW_EN) indicates that memory addresses within the base and limit addresses are mapped to a specific traffic class ID. Bits 3:1 (TC_ID) identify the specific traffic class ID. **Note:** Memory-mapped register space exists for four upstream windows. Only window 0 is included in this table.
Device control memory window register 0Ch	Upstream isochronous window 0 base address (see Section 6.6)	Window 0 base address
Device control memory window register 10h	Upstream isochronous window 0 limit address (see Section 6.7)	Window 0 limit address

Not Recommended for New Designs

3.4.3 PCI Express Extended VC With VC Arbitration

When a second VC is enabled, the bridge has three arbitration options that determine which VC is granted access to the upstream PCI Express link. These three arbitration modes include strict priority, hardware-fixed round-robin, and 32-phase WRR. The default mode is strict priority. For all three arbitration modes, if the second VC is disabled, then VC0 is always granted.

To map upstream transactions to the extended VC, the following registers must be programmed:

1. Bit 0 (ISOC_ENABLE) is asserted in the upstream isochrony control register at device control memory window register offset 04h (see Section 6.4).
2. At least one PCI isochronous window register set must be programmed. Please see Section 3.4.2 for a description on how to program this advanced feature.
3. The traffic class ID selected for the PCI isochronous window(s) must be assigned to the extended VC. This is accomplished by asserting the corresponding bit in the TC_VC_MAP field in the VC resource control register (VC1) at PCI Express extended register offset 170h (see Section 5.25).
4. The extended VC must be enabled. This is accomplished by asserting bit 31 (VC_EN) and programming bits 26:24 (VC_ID) in the VC resource control register (VC1) at PCI Express extended register offset 170h.

3.4.3.1 Strict Priority Arbitration Mode

Strict priority arbitration always grants VC1 traffic over VC0 traffic. If the traffic on VC1 uses 100% of the upstream link bandwidth, then VC0 traffic is blocked. This mode is enabled when bit 25 (STRICT_PRIORITY_EN) in the general control register at offset D4h equals 1b (see Section 4.65).

For applications that require QoS or isochronous operation, this arbitration mode is recommended. In this mode, all traffic on VC1 is assured access to the upstream link and VC0 traffic is best effort with a lower priority.

3.4.3.2 Hardware-Fixed, Round-Robin Arbitration

Hardware-fixed, round-robin arbitration alternates between VC0 and the second VC. Over an extended period of time, if both VCs are heavily loaded with equal data payloads, then each VC is granted approximately 50% of the upstream link bandwidth. The PCI configuration registers described in Table 3–8 configure the hardware-fixed, round-robin arbitration mode.

Table 3–8. Hardware-Fixed, Round-Robin Arbiter Registers

PCI OFFSET	REGISTER NAME	DESCRIPTION
Classic PCI configuration register D4h	General control (see Section 4.65)	Bit 25 (STRICT_PRIORITY_EN) equal to 0b enables either hardware-fixed, round-robin or 32-phase, WRR arbitration mode.
Classic PCI configuration register 15Ch	Port VC control (see Section 5.19)	Bits 3:1 (VC_ARB_SELECT) equal to 000b enable hardware-fixed, round-robin arbitration mode.

3.4.3.3 32-Phase, WRR Arbitration Mode

When the second upstream VC is enabled, the VC arbiter selects the next PCI Express upstream link transaction based on entries within a VC arbitration table. There are actually two VC arbitration tables within the bridge. The first table is accessed through the extended PCI Express configuration register space using configuration read/write transactions. The second table is internal and is used by the VC arbiter to make selection decisions. A configuration register load function exists to transfer the contents of the configuration register table to the internal table.

The VC arbitration table uses a 4-bit field to identify the VC that is selected during each arbiter cycle. Bits 2:0 of this 4-bit field are loaded with the VC_ID assigned to each VC. For the arbiter to recognize a VC request, the software must allocate only 1 phase to the same VC_ID.

The PCI configuration registers described in Table 3–9 configure the 32-phase, WRR arbitration mode.

Not Recommended for New Designs

Table 3–9. 32-Phase, WRR Arbiter Registers

PCI OFFSET	REGISTER NAME	DESCRIPTION
Classic PCI configuration register D4h	General control (see Section 4.65)	Bit 25 (STRICT_PRIORITY_EN) equal to 0b enables either hardware-fixed, round-robin or 32-phase, WRR arbitration mode.
PCI Express VC extended configuration register 15Ch	Port VC control (see Section 5.19)	Bit 0 (LOAD_VC_TABLE) when written with a 1b transfers the VC arbitration table configuration register values to the internal registers used by the VC arbiter. Bits 3:1 (VC_ARB_SELECT) equal to 001b enable the 32-phase, WRR arbitration mode.
PCI Express VC extended configuration register 15Eh	Port VC status (see Section 5.20)	Bit 0 (VC_TABLE_STATUS) equal to 1b indicates that the VC arbitration table configuration registers were updated but not loaded into the internal arbitration table.
PCI Express VC extended configuration registers 180h to 18Ch	VC arbitration table (see Section 5.27)	4-doubleword sized configuration registers that are the registered version of the 32-phase, WRR VC arbitration table. Each VC arbitration table entry is a 4-bit field.

3.4.4 128-Phase, WRR PCI Port Arbitration Timing

This section includes a timing diagram that illustrates the 128-phase, WRR time-based arbiter timing for the bridge and 1394a OHCI devices. This timing diagram assumes aggressive mode since the transfer associated with the bridge is stopped to start a 1394a OHCI transaction. The PCI bus cycle where the bridge is stopped is indicated by the ‡ symbol. The bridge then waits until its next port arbitration table cycle to finish the transfer.

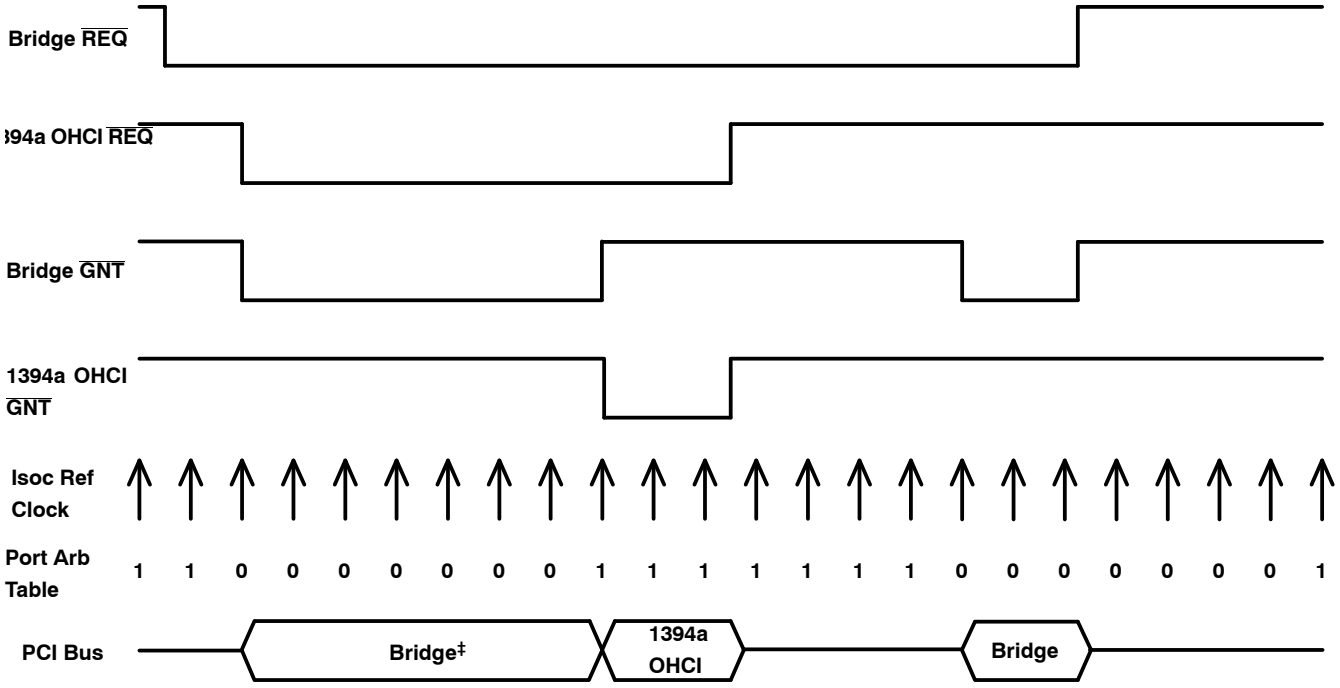

Figure 3–4. Internal PCI Bus Timing

Not Recommended for New Designs

3.5 PCI Interrupt Conversion to PCI Express Messages

The bridge converts interrupts from the PCI bus sideband interrupt signals to PCI Express interrupt messages. Since the 1394a OHCI only generates $\overline{\text{INTA}}$ interrupts, only PCI Express INTA messages are generated by the bridge.

PCI Express Assert_INTA messages are generated when the 1394a OHCI signals an $\overline{\text{INTA}}$ interrupt. The requester ID portion of the Assert_INTA message uses the value stored in the primary bus number register (see Section 4.11) as the bus number, 0 as the device number, and 0 as the function number. The tag field for each Assert_INTA message is 00h.

PCI Express Deassert_INTA messages are generated when the 1394a OHCI deasserts the $\overline{\text{INTA}}$ interrupt. The requester ID portion of the Deassert_INTA message uses the value stored in the primary bus number register as the bus number, 0 as the device number, and 0 as the function number. The Tag field for each Deassert_INTA message is 00h.

Figure 3–5 and Figure 3–6 illustrate the format for both the assert and deassert INTA messages.

	+0								+1								+2								+3							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Byte 0>	R	Fmt		Type					R	TC			Reserved				T D	E P	Attr		R		Length									
		0	1	1	0	1	0	0		0	0	0							0	0			0	0	0	0	0	0	0	0	0	0
Byte 4>	Requester ID																Tag								Code							
																									0	0	1	0	0	0	0	0
Byte 8> Byte 12>	Reserved																															

Figure 3–5. PCI Express ASSERT_INTA Message

	+0								+1								+2								+3							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Byte 0>	R	Fmt		Type					R	TC			Reserved				T D	E P	Attr		R		Length									
		0	1	1	0	1	0	0		0	0	0							0	0			0	0	0	0	0	0	0	0	0	0
Byte 4>	Requester ID																Tag								Code							
																									0	0	1	0	0	1	0	0
Byte 8> Byte 12>	Reserved																															

Figure 3–6. PCI Express DEASSERT_INTX Message

3.6 Two-Wire Serial-Bus Interface

The bridge provides a two-wire serial-bus interface to load subsystem identification information and specific register defaults from an external EEPROM. The serial-bus interface signals (SCL and SDA) are shared with two of the GPIO terminals (4 and 5). If the serial bus interface is enabled, then the GPIO4 and GPIO5 terminals are disabled. If the serial bus interface is disabled, then the GPIO terminals operate as described in Section 3.9.

3.6.1 Serial-Bus Interface Implementation

To enable the serial-bus interface, a pullup resistor must be implemented on the SDA signal. At the rising edge of $\overline{\text{PERST}}$ or $\overline{\text{GRST}}$, whichever occurs later in time, the SDA terminal is checked for a pullup resistor. If one is detected, then bit 3 (SBDETECT) in the serial-bus control and status register (see Section 4.58) is set. Software may disable the serial-bus interface at any time by writing a 0b to the SBDETECT bit. If no external EEPROM is required, then the serial-bus interface is permanently disabled by attaching a pulldown resistor to the SDA signal.

The bridge implements a two-terminal serial interface with one clock signal (SCL) and one data signal (SDA). The SCL signal is a unidirectional output from the bridge and the SDA signal is bidirectional. Both are open-drain signals and require pullup resistors. The bridge is a bus master device and drives SCL at approximately 60 kHz during data transfers and places SCL in a high-impedance state (0 frequency) during bus idle states. The serial EEPROM is a bus slave device and must acknowledge a slave address equal to A0h. Figure 3–7 illustrates an example application implementing the two-wire serial bus.

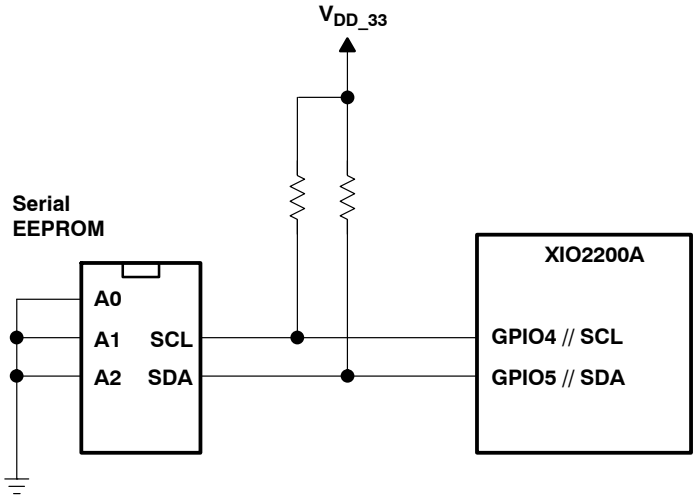

Figure 3–7. Serial EEPROM Application

3.6.2 Serial-Bus Interface Protocol

All data transfers are initiated by the serial-bus master. The beginning of a data transfer is indicated by a start condition, which is signaled when the SDA line transitions to the low state while SCL is in the high state, as illustrated in Figure 3–8. The end of a requested data transfer is indicated by a stop condition, which is signaled by a low-to-high transition of SDA while SCL is in the high state, as shown in Figure 3–8. Data on SDA must remain stable during the high state of the SCL signal, as changes on the SDA signal during the high state of SCL are interpreted as control signals, that is, a start or stop condition.

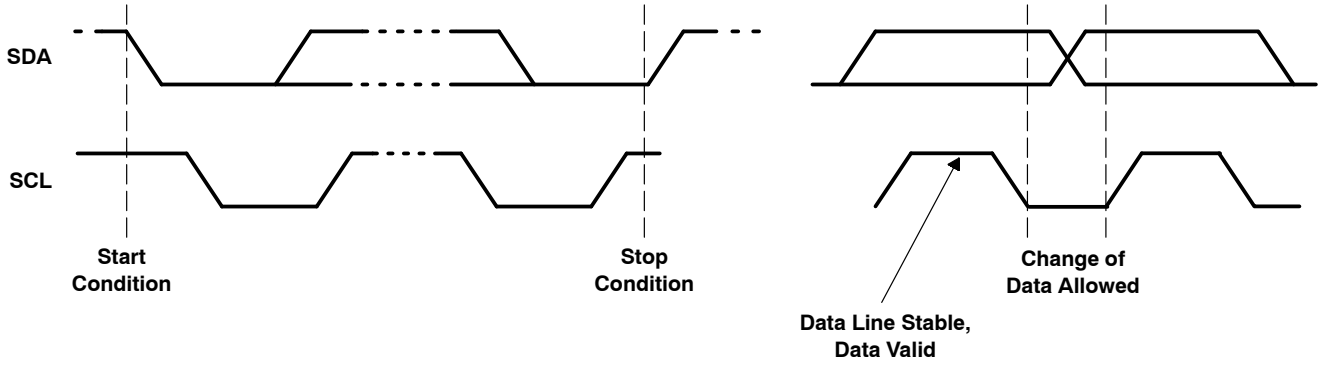

Figure 3–8. Serial-Bus Start/Stop Conditions and Bit Transfers

Data is transferred serially in 8-bit bytes. During a data transfer operation, the exact number of bytes that are transmitted is unlimited. However, each byte must be followed by an acknowledge bit to continue the data transfer operation. An acknowledge (ACK) is indicated by the data byte receiver pulling the SDA signal low, so that it remains low during the high state of the SCL signal. Figure 3–9 illustrates the acknowledge protocol.

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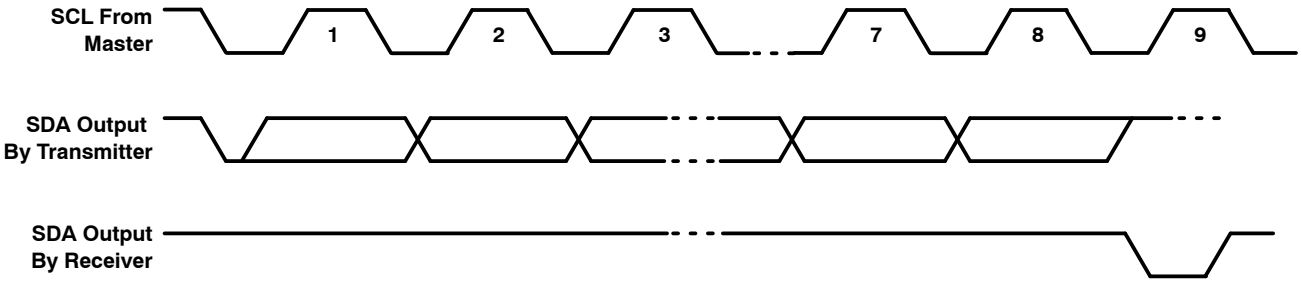

Figure 3–9. Serial-Bus Protocol Acknowledge

The bridge performs three basic serial-bus operations: single byte reads, single byte writes, and multibyte reads. The single byte operations occur under software control. The multibyte read operations are performed by the serial EEPROM initialization circuitry immediately after a PCI Express reset. See Section 3.6.3, *Serial-Bus EEPROM Application*, for details on how the bridge automatically loads the subsystem identification and other register defaults from the serial-bus EEPROM.

Figure 3–10 illustrates a single byte write. The bridge issues a start condition and sends the 7-bit slave device address and the R/$\overline{W}$ command bit is equal to 0b. A 0b in the R/$\overline{W}$ command bit indicates that the data transfer is a write. The slave device acknowledges if it recognizes the slave address. If no acknowledgment is received by the bridge, then bit 1 (SB_ERR) is set in the serial-bus control and status register (PCI offset B3h, see Section 4.58). Next, the EEPROM word address is sent by the bridge, and another slave acknowledgment is expected. Then the bridge delivers the data byte MSB first and expects a final acknowledgment before issuing the stop condition.

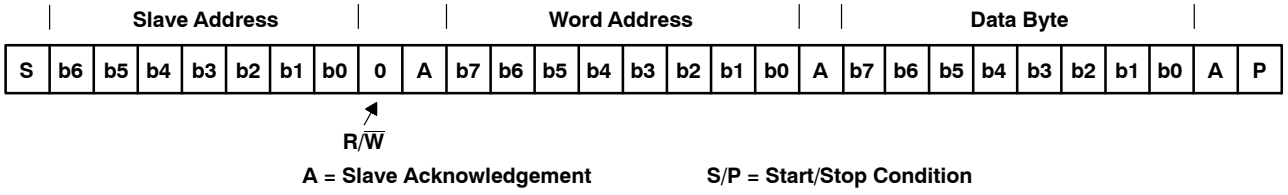

Figure 3–10. Serial-Bus Protocol—Byte Write

Figure 3–11 illustrates a single byte read. The bridge issues a start condition and sends the 7-bit slave device address and the R/$\overline{W}$ command bit is equal to 0b (write). The slave device acknowledges if it recognizes the slave address. Next, the EEPROM word address is sent by the bridge, and another slave acknowledgment is expected. Then, the bridge issues a restart condition followed by the 7-bit slave address and the R/$\overline{W}$ command bit is equal to 1b (read). Once again, the slave device responds with an acknowledge. Next, the slave device sends the 8-bit data byte, MSB first. Since this is a 1-byte read, the bridge responds with no acknowledge (logic high) indicating the last data byte. Finally, the bridge issues a stop condition.

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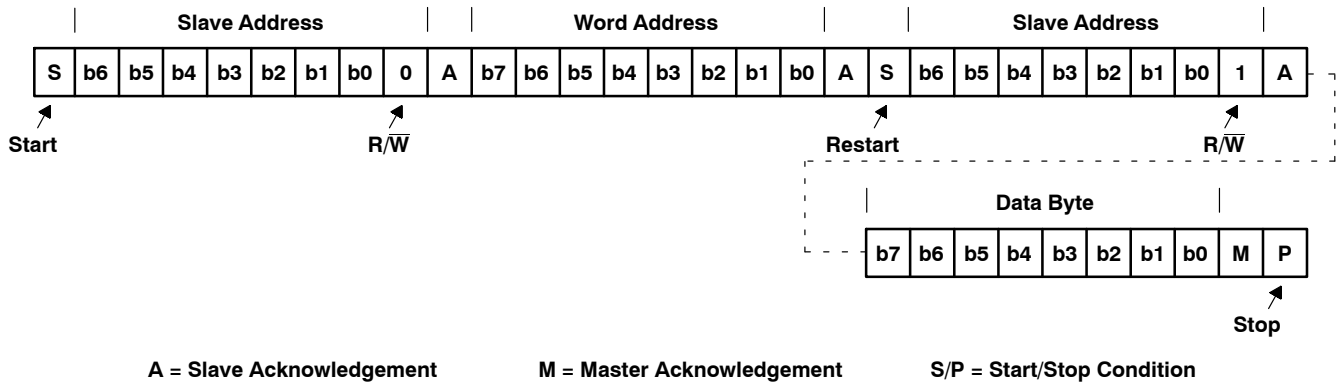

Figure 3–11. Serial-Bus Protocol—Byte Read

Figure 3–12 illustrates the serial interface protocol during a multi-byte serial EEPROM download. The serial-bus protocol starts exactly the same as a 1-byte read. The only difference is that multiple data bytes are transferred. The number of transferred data bytes is controlled by the bridge master. After each data byte, the bridge master issues acknowledge (logic low) if more data bytes are requested. The transfer ends after a bridge master no acknowledge (logic high) followed by a stop condition.

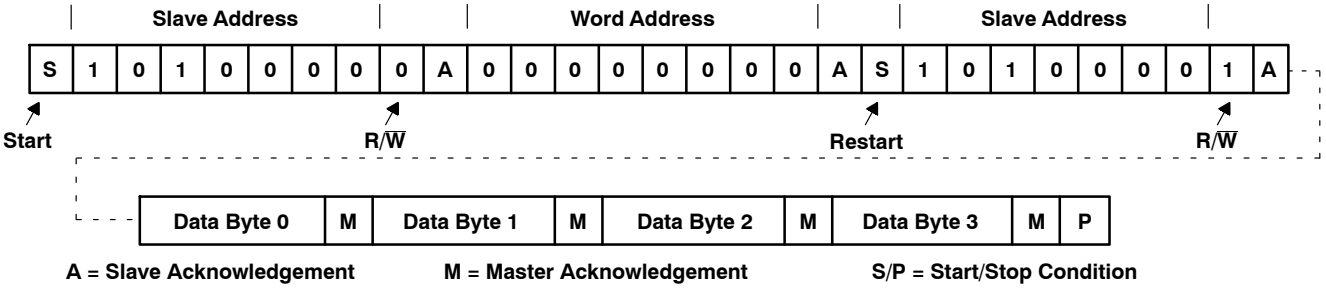

Figure 3–12. Serial-Bus Protocol—Multibyte Read

Bit 7 (PROT_SEL) in the serial-bus control and status register changes the serial-bus protocol. Each of the three previous serial-bus protocol figures illustrates the PROT_SEL bit default (logic low). When this control bit is asserted, the word address and corresponding acknowledge are removed from the serial-bus protocol. This feature allows the system designer a second serial-bus protocol option when selecting external EEPROM devices.

3.6.3 Serial-Bus EEPROM Application

The registers and corresponding bits that are loaded through the EEPROM are provided in Table 3–10.

Not Recommended for New Designs

Table 3–10. EEPROM Register Loading Map

SERIAL EEPROM WORD ADDRESS	BYTE DESCRIPTION	
00h	PCI-Express to PCI bridge function indicator (00h)	
01h	Number of bytes to download (1Eh)	
02h	PCI 84h, subsystem vendor ID, byte 0	
03h	PCI 85h, subsystem vendor ID, byte 1	
04h	PCI 86h, subsystem ID, byte 0	
05h	PCI 87h, subsystem ID, byte 1	
06h	PCI D4h, general control, byte 0	
07h	PCI D5h, general control, byte 1	
08h	PCI D6h, general control, byte 2	
09h	PCI D7h, general control, byte 3	
0Ah	TI Proprietary register load 00h (PCI D8h)	
0Bh	TI Proprietary register load 00h (PCI D9h)	
0Ch	Reserved—no bits loaded	
0Dh	PCI DCh, arbiter control	
0Eh	PCI DDh, arbiter request mask	
0Fh	PCI C0h, control and diagnostic register 0 byte 0	
10h	PCI C1h, control and diagnostic register 0 byte 1	
11h	PCI C2h, control and diagnostic register 0 byte 2	
12h	PCI C3h, control and diagnostic register 0 byte 3	
13h	PCI C4h, control and diagnostic register 1 byte 0	
14h	PCI C5h, control and diagnostic register 1 byte 1	
15h	PCI C6h, control and diagnostic register 1 byte 2	
16h	PCI C7h, control and diagnostic register 1 byte 3	
17h	PCI C8h, control and diagnostic register 2 byte 0	
18h	PCI C9h, control and diagnostic register 2 byte 1	
19h	PCI CAh, control and diagnostic register 2 byte 2	
1Ah	PCI CBh, control and diagnostic register 2 byte 3	
1Bh	Reserved—no bits loaded	
1Ch	Reserved—no bits loaded	
1Dh	TI Proprietary register load 00h (PCI E0h)	
1Eh	TI Proprietary register load 00h (PCI E2h)	
1Fh	TI Proprietary register load 00h (PCI E3h)	
20h	1394 OHCI function indicator (01h)	
21h	Number of bytes (17h)	
22h	PCI 3Fh, maximum latency, bits 7–4	PCI 3Eh, minimum grant, bits 3–0
23h	PCI 2Ch, subsystem vendor ID, byte 0	
24h	PCI 2Dh, subsystem vendor ID, byte 1	
25h	PCI 2Eh, subsystem ID, byte 0	
26h	PCI 2Fh, subsystem ID, byte 1	

Not Recommended for New Designs

Table 3–10. EEPROM Register Loading Map (Continued)

SERIAL EEPROM WORD ADDRESS	BYTE DESCRIPTION					
27h	PCI F4h, Link_Enh, byte 0, bits 7, 2, 1 OHCI 50h, host controller control, bit 23					
	[7] Link_Enh enab_unfair	[6] HC Control Program Phy Enable	[5:3] RSVD	[2] Link_Enh bit 2	[1] Link_Enh enab_accel	[0] RSVD
28h	Mini–ROM Address, this byte indicates the MINI ROM offset into the EEPROM 00h = No MINI ROM 01h to FFh = MINI ROM offset					
29h	OHCI 24h, GUIDHi, byte 0					
2Ah	OHCI 25h, GUIDHi, byte 1					
2Bh	OHCI 26h, GUIDHi, byte 2					
2Ch	OHCI 27h, GUIDHi, byte 3					
2Dh	OHCI 28h, GUIDLo, byte 0					
2Eh	OHCI 29h, GUIDLo, byte 1					
2Fh	OHCI 2Ah, GUIDLo, byte 2					
30h	OHCI 2Bh, GUIDLo, byte 3					
31h	Reserved—No bits loaded					
32h	PCI F5h, Link_Enh, byte 1, bits 7, 6, 5, 4					
33h	PCI F0h, PCI miscellaneous, byte 0, bits 7, 4, 2, 1, 0					
34h	PCI F1h, PCI miscellaneous, byte 1, bits 1, 0					
35h	Reserved—No bits loaded					
36h	Reserved—No bits loaded					
37h	Reserved—No bits loaded					
38h	PCI ECh, PCI PHY control, bits 7, 3, 1					
39h	End-of-list indicator (80h)					

This format must be explicitly followed for the bridge to correctly load initialization values from a serial EEPROM. All byte locations must be considered when programming the EEPROM.

The serial EEPROM is addressed by the bridge at slave address 1010 000b. This slave address is internally hardwired and cannot be changed by the system designer. Therefore, all three hardware address bits for the EEPROM are tied to V_{SS} to achieve this address. The serial EEPROM in the sample application circuit (Figure 3–7) assumes the 1010b high-address nibble. The lower three address bits are terminal inputs to the chip, and the sample application shows these terminal inputs tied to V_{SS}.

During an EEPROM download operation, bit 4 (ROMBUSY) in the serial-bus control and status register is asserted. After the download is finished, bit 0 (ROM_ERR) in the serial-bus control and status register may be monitored to verify a successful download.

3.6.4 Accessing Serial-Bus Devices Through Software

The bridge provides a programming mechanism to control serial-bus devices through system software. The programming is accomplished through a doubleword of PCI configuration space at offset B0h. Table 3–11 lists the registers that program a serial-bus device through software.

Not Recommended for New Designs

Table 3–11. Registers Used To Program Serial-Bus Devices

PCI OFFSET	REGISTER NAME	DESCRIPTION
B0h	Serial-bus data (see Section 4.55)	Contains the data byte to send on write commands or the received data byte on read commands.
B1h	Serial-bus word address (see Section 4.56)	The content of this register is sent as the word address on byte writes or reads. This register is not used in the quick command protocol. Bit 7 (PROT_SEL) in the serial-bus control and status register (offset B3h, see Section 4.58) is set to 1b to enable the slave address to be sent.
B2h	Serial-bus slave address (see Section 4.57)	Write transactions to this register initiate a serial-bus transaction. The slave device address and the R/$\overline{W}$ command selector are programmed through this register.
B3h	Serial-bus control and status (see Section 4.58)	Serial interface enable, busy, and error status are communicated through this register. In addition, the protocol-select bit (PROT_SEL) and serial-bus test bit (SBTEST) are programmed through this register.

To access the serial EEPROM through the software interface, the following steps are performed:

1. The control and status byte is read to verify the EEPROM interface is enabled (SBDETECT asserted) and not busy (REQBUSY and ROMBUSY deasserted).
2. The serial-bus word address is loaded. If the access is a write, then the data byte is also loaded.
3. The serial-bus slave address and R/$\overline{W}$ command selector byte is written.
4. REQBUSY is monitored until this bit is deasserted.
5. SB_ERR is checked to verify that the serial-bus operation completed without error. If the operation is a read, then the serial-bus data byte is now valid.

3.7 Advanced Error Reporting Registers

In the extended PCI Express configuration space, the bridge supports the advanced error reporting capabilities structure. For the PCI Express interface, both correctable and uncorrectable error statuses are provided. For the PCI bus interface, secondary uncorrectable error status is provided. All uncorrectable status bits have corresponding mask and severity control bits. For correctable status bits, only mask bits are provided.

Both the primary and secondary interfaces include first error pointer and header log registers. When the first error is detected, the corresponding bit position within the uncorrectable status register is loaded into the first error pointer register. Likewise, the header information associated with the first failing transaction is loaded into the header log. To reset this first error control logic, the corresponding status bit in the uncorrectable status register is cleared by a writeback of 1b.

For systems that require high data reliability, ECRC is fully supported on the PCI Express interface. The primary side advanced error capabilities and control register has both ECRC generation and checking enable control bits. When the checking bit is asserted, all received TLPs are checked for a valid ECRC field. If the generation bit is asserted, then all transmitted TLPs contain a valid ECRC field.

3.8 Data Error Forwarding Capability

The bridge supports the transfer of data errors in both directions.

If a downstream PCI Express transaction with a data payload is received that targets the internal PCI bus and the EP bit is set indicating poisoned data, then the bridge must ensure that this information is transferred to the PCI bus. To do this, the bridge forces a parity error on each PCI bus data phase by inverting the parity bit calculated for each double-word of data.

If the bridge is the target of a PCI transaction that is forwarded to the PCI Express interface and a data parity error is detected, then this information is passed to the PCI Express interface. To do this, the bridge sets the EP bit in the upstream PCI Express header.

Not Recommended for New Designs

3.9 General-Purpose I/O Interface

Up to eight general-purpose input/output (GPIO) terminals are provided for system customization. These GPIO terminals are 3.3-V tolerant.

The exact number of GPIO terminals varies based on implementing the clock run, power override, and serial EEPROM interface features. These features share four of the eight GPIO terminals. When any of the three shared functions are enabled, the associated GPIO terminal is disabled.

All eight GPIO terminals are individually configurable as either inputs or outputs by writing the corresponding bit in the GPIO control register at offset B4h. A GPIO data register at offset B6h exists to either read the logic state of each GPIO input or to set the logic state of each GPIO output. The power-up default state for the GPIO control register is input mode.

3.10 Set Slot Power Limit Functionality

The *PCI Express Specification* provides a method for devices to limit internal functionality and save power based on the value programmed into the captured slot power limit scale (CSPLS) and capture slot power limit value (CSPLV) fields of the PCI Express device capabilities register at offset 94h. See Section 4.49, *Device Capabilities Register*, for details. The bridge writes these fields when a set slot power limit message is received on the PCI Express interface.

After the deassertion of $\overline{\text{PERST}}$, the XIO2200A compares the information within the CSPLS and CSPLV fields of the device capabilities register to the minimum power scale (MIN_POWER_SCALE) and minimum power value (MIN_POWER_VALUE) fields in the general control register at offset D4h. See Section 4.65, *General Control Register*, for details. If the CSPLS and CSPLV fields are less than the MIN_POWER_SCALE and MIN_POWER_VALUE fields, respectively, then the bridge takes the appropriate action that is defined below.

The power usage action is programmable within the bridge. The general control register includes a 3-bit PWR_OVRD field. This field is programmable to the following two options:

1. Ignore slot power limit fields
2. Respond with unsupported request to all transactions except type 0/1 configuration transactions and set slot power limit messages

3.11 PCI Express and PCI Bus Power Management

The bridge supports both software-directed power management and active state power management through standard PCI configuration space. Software-directed registers are located in the power management capabilities structure located at offset 50h. Active state power management control registers are located in the PCI Express capabilities structure located at offset 90h.

During software-directed power management state changes, the bridge initiates link state transitions to L1 or L2/L3 after a configuration write transaction places the device in a low power state. The power management state machine is also responsible for gating internal clocks based on the power state. Table 3–12 identifies the relationship between the D-states and bridge clock operation.

Table 3–12. Clocking In Low Power States

CLOCK SOURCE	D0/L0	D1/L1	D2/L1	D3/L2/L3
PCI express reference clock input (REFCLK)	On	On	On	On/Off
Internal PCI bus clock to bridge function	On	Off	Off	Off
Internal PCI bus clock to 1394a OHCI function	On	On	On	On/Off

The link power management (LPM) state machine manages active state power by monitoring the PCI Express transaction activity. If no transactions are pending and the transmitter has been idle for at least the minimum time required by the *PCI Express Specification*, then the LPM state machine transitions the link to either the L0s or L1 state. By reading the bridge's L0s and L1 exit latency in the link capabilities register, the system software may make an informed decision relating to system performance versus power savings. The ASLPMC field in the link control register provides an L0s only option, L1 only option, or both L0s and L1 option.

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Finally, the bridge generates the PM_Active_State_Nak Message if a PM_Active_State_Request_L1 DLLP is received on the PCI Express interface and the link cannot be transitioned to L1.

3.12 1394a OHCI Controller Functionality

3.12.1 1394a OHCI Power Management

The 1394a OHCI controller complies with the *PCI Bus Power Management Interface Specification*. The controller supports the D0 (uninitialized), D0 (active), D1, D2, and D3 power states as defined by the power management definition in the *1394 Open Host Controller Interface Specification*, Appendix A4.

Table 3–13 identifies the supported power management registers within the 1394a OHCI configuration register map.

Table 3–13. 1394a OHCI Configuration Register Map

REGISTER NAME				OFFSET
Power management capabilities		Next item pointer	Capability ID	44h
PM data	Power management control/status register bridge support extensions	Power management control/status (CSR)		48h

3.12.2 1394a OHCI and V_{AUX}

The 1394a OHCI function within the XIO2200A is powered by V_{DD_MAIN} only. Therefore, during the $D3_{cold}$ power management state, V_{AUX} is not supplied to the 1394a OHCI function.

This implies that the 1394a OHCI function does not implement sticky bits and needs to be initialized after a $D3_{cold}$ power management state. An external serial EEPROM interface is available to initialize critical configuration register bits. The EEPROM download is triggered by the deassertion of the $\overline{PERST}$ input. Otherwise, the BIOS will need to initialize the 1394a OHCI function.

3.12.3 1394a OHCI and Reset Options

The 1394a OHCI function is completely reset by the internal power-on reset feature, by the $\overline{GRST}$ input, or by the PCI Express reset ($\overline{PERST}$) input. This includes all EEPROM loadable bits, power management functions, and all remaining configuration register bits and logic.

A PCI Express training control hot reset or the PCI bus configuration register reset bit (SRST) excludes the EEPROM loadable bits, power management functions, and 1394 PHY. All remaining configuration registers and logic are reset.

If the OHCI controller is in the power management D2 or D3 state or if the OHCI configuration register reset bit (SoftReset) is set, the OHCI controller DMA logic and link logic is reset.

Finally, if the OHCI configuration register PHY reset bit (ISBR) is set, the 1394 PHY logic is reset.

3.12.4 1394a OHCI PCI Bus Master

As a bus master, the 1394 OHCI function supports the memory commands specified in Table 3–14. The commands include memory read, memory read line, memory read multiple, memory write, and memory write and invalidate.

The read command usage for read transactions of greater than two data phases are determined by the selection in bits 9:8 (MR_ENHANCE field) of the PCI miscellaneous configuration register at offset F0h (see Section 7.22). For read transactions of one or two data phases, a memory read command is used.

The write command usage is determined by the MWI_ENB bit 4 of the command configuration register at offset 04h (see Section 4.3). If bit 4 is asserted and a memory write starts on a cache boundary with a length greater than one cache line, then memory write and invalidate commands are used. Otherwise, memory write commands are used.

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Table 3–14. 1394a OHCI Memory Command Options

PCI	COMMAND C/BE3–C/BE0	OHCI MASTER FUNCTION
Memory read	0110	DMA read from memory
Memory write	0111	DMA write to memory
Memory read multiple	1100	DMA read from memory
Memory read line	1110	DMA read from memory
Memory write and invalidate	1111	DMA write to memory

3.12.5 1394a OHCI Subsystem Identification

The subsystem identification register at offset 2Ch is used for system and option card identification purposes. This register can be initialized from the serial EEPROM or programmed via the subsystem access register at offset F8h in the 1394a OHCI PCI configuration space (see Section 7.24).

Write access to the subsystem access register updates the subsystem identification registers identically to OHCI-Lynx™. The contents of the subsystem access register are aliased to the subsystem vendor ID and subsystem ID registers at PCI offsets 2Ch and 2Eh, respectively. The subsystem ID value written to this register may also be read back from this register.

3.12.6 1394a OHCI PME Support

Since the 1394a OHCI controller is not connected to VAUX, PME generation is disabled for $D3_{cold}$ power management states.

Not Recommended for New Designs

4 Classic PCI Configuration Space

The programming model of the XIO2200A PCI-Express to PCI bridge is compliant to the classic PCI-to-PCI bridge programming model. The PCI configuration map uses the type 1 PCI bridge header.

All bits marked with a ☆ are sticky bits and are reset by a global reset ($\overline{GRST}$) or the internally-generated power-on reset. All bits marked with a † are reset by a PCI Express reset ($\overline{PERST}$), a $\overline{GRST}$, or the internally-generated power-on reset. The remaining register bits are reset by a PCI Express hot reset, $\overline{PERST}$, $\overline{GRST}$, or the internally-generated power-on reset.

Table 4–1. Classic PCI Configuration Register Map

REGISTER NAME				OFFSET
Device ID		Vendor ID		000h
Status		Command		004h
Class code			Revision ID	008h
BIST	Header type	Latency timer	Cache line size	00Ch
Device control base address				010h
Reserved				014h
Secondary latency timer	Subordinate bus number	Secondary bus number	Primary bus number	018h
Secondary status		I/O limit	I/O base	01Ch
Memory limit		Memory base		020h
Prefetchable memory limit		Prefetchable memory base		024h
Prefetchable base upper 32 bits				028h
Prefetchable limit upper 32 bits				02Ch
I/O limit upper 16 bits		I/O base upper 16 bits		030h
Reserved			Capabilities pointer	034h
Reserved				038h
Bridge control		Interrupt pin	Interrupt line	03Ch
Reserved				040h–04Ch
Power management capabilities		Next item pointer	PM capability ID	050h
PM data	PMCSR_BSE	Power management CSR		054h
Reserved				058h–05Ch
MSI message control		Next item pointer	MSI CAP ID	060h
MSI message address				064h
MSI upper message address				068h
Reserved		MSI message data		06Ch
Reserved				070h–07Ch
Reserved		Next item pointer	SSID/SSVID capability ID	080h
Subsystem ID†		Subsystem vendor ID†		084h
Reserved				088h–08Ch
PCI Express capabilities register		Next item pointer	PCI Express capability ID	090h
Device capabilities				094h
Device status		Device control		098h
Link capabilities				09Ch
Link status		Link control		0A0h
Reserved				0A4h–0ACh
Serial-bus control and status†	Serial-bus slave address†	Serial-bus word address†	Serial-bus data†	0B0h

† One or more bits in this register are reset by a PCI Express reset ($\overline{PERST}$), a $\overline{GRST}$, or the internally-generated power-on reset.

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Table 4–1. PCI Express Configuration Register Map (Continued)

REGISTER NAME				OFFSET
GPIO data†		GPIO control†		0B4h
Reserved				0B8h–0BCh
Control and diagnostic register 0†				0C0h
Control and diagnostic register 1†				0C4h
Control and diagnostic register 2†				0C8h
Reserved				0CCh
Subsystem access†				0D0h
General control†				0D4h
Reserved	TI proprietary†	TI proprietary†	TI proprietary†	0D8h
Reserved	Arbiter time-out status	Arbiter request mask†	Arbiter control†	0DCh
TI proprietary†		Reserved	TI proprietary†	0E0h
Reserved		TI proprietary		0E4h
Reserved				0E8h–0FCh

† One or more bits in this register are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

4.1 Vendor ID Register

This 16-bit read-only register contains the value 104Ch, which is the vendor ID assigned to Texas Instruments.

PCI register offset: 00h
Register type: Read-only
Default value: 104Ch

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	1	0	0	0	0	0	1	0	0	1	1	0	0

4.2 Device ID Register

This 16-bit read-only register contains the value 8231h, which is the device ID assigned by TI for the bridge.

PCI register offset: 02h
Register type: Read-only
Default value: 8231h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	1	0	0	0	0	0	1	0	0	0	1	1	0	0	0	1

Not Recommended for New Designs

4.3 Command Register

The command register controls how the bridge behaves on the PCI Express interface. See Table 4–2 for a complete description of the register contents.

PCI register offset: 04h
Register type: Read-only, Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4–2. Command Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:11	RSVD	R	Reserved. Returns 00000b when read.
10	INT_DISABLE	R	$\overline{\text{INTx}}$ disable. This bit enables device specific interrupts. Since the bridge does not generate any internal interrupts, this bit is read-only 0b.
9	FBB_ENB	R	Fast back-to-back enable. The bridge does not generate fast back-to-back transactions; therefore, this bit returns 0b when read.
8	SERR_ENB	RW	$\overline{\text{SERR}}$ enable bit. When this bit is set, the bridge can signal fatal and nonfatal errors on the PCI Express interface on behalf of $\overline{\text{SERR}}$ assertions detected on the PCI bus. 0 = Disable the reporting of nonfatal errors and fatal errors (default) 1 = Enable the reporting of nonfatal errors and fatal errors
7	STEP_ENB	R	Address/data stepping control. The bridge does not support address/data stepping, and this bit is hardwired to 0b.
6	PERR_ENB	RW	Controls the setting of bit 8 (DATAPAR) in the status register (offset 06h, see Section 4.4) in response to a received poisoned TLP from PCI Express. A received poisoned TLP is forwarded with bad parity to conventional PCI regardless of the setting of this bit. 0 = Disables the setting of the master data parity error bit (default) 1 = Enables the setting of the master data parity error bit
5	VGA_ENB	R	VGA palette snoop enable. The bridge does not support VGA palette snooping; therefore, this bit returns 0b when read.
4	MWI_ENB	RW	Memory write and invalidate enable. When this bit is set, the bridge translates PCI Express memory write requests into memory write and invalidate transactions on the PCI interface. 0 = Disable the promotion to memory write and invalidate (default) 1 = Enable the promotion to memory write and invalidate
3	SPECIAL	R	Special cycle enable. The bridge does not respond to special cycle transactions; therefore, this bit returns 0b when read.
2	MASTER_ENB	RW	Bus master enable. When this bit is set, the bridge is enabled to initiate transactions on the PCI Express interface. 0 = PCI Express interface cannot initiate transactions. The bridge must disable the response to memory and I/O transactions on the PCI interface (default). 1 = PCI Express interface can initiate transactions. The bridge can forward memory and I/O transactions from PCI secondary interface to the PCI Express interface.
1	MEMORY_ENB	RW	Memory space enable. Setting this bit enables the bridge to respond to memory transactions on the PCI Express interface. 0 = PCI Express receiver cannot process downstream memory transactions and must respond with an unsupported request (default) 1 = PCI Express receiver can process downstream memory transactions. The bridge can forward memory transactions to the PCI interface.
0	IO_ENB	RW	I/O space enable. Setting this bit enables the bridge to respond to I/O transactions on the PCI Express interface. 0 = PCI Express receiver cannot process downstream I/O transactions and must respond with an unsupported request (default) 1 = PCI Express receiver can process downstream I/O transactions. The bridge can forward I/O transactions to the PCI interface.

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4.4 Status Register

The status register provides information about the PCI Express interface to the system. See Table 4–3 for a complete description of the register contents.

PCI register offset: 06h
Register type: Read-only, Read/Clear
Default value: 0010h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Table 4–3. Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15	PAR_ERR	RCU	Detected parity error. This bit is set when the PCI Express interface receives a poisoned TLP. This bit is set regardless of the state of bit 6 (PERR_ENB) in the command register (offset 04h, see Section 4.3). 0 = No parity error detected 1 = Parity error detected
14	SYS_ERR	RCU	Signaled system error. This bit is set when the bridge sends an ERR_FATAL or ERR_NONFATAL message and bit 8 (SERR_ENB) in the command register (offset 04h, see Section 4.3) is set. 0 = No error signaled 1 = ERR_FATAL or ERR_NONFATAL signaled
13	MABORT	RCU	Received master abort. This bit is set when the PCI Express interface of the bridge receives a completion-with-unsupported-request status. 0 = Unsupported request not received on the PCI Express interface 1 = Unsupported request received on the PCI Express interface
12	TABORT_REC	RCU	Received target abort. This bit is set when the PCI Express interface of the bridge receives a completion-with-completer-abort status. 0 = Completer abort not received on the PCI Express interface 1 = Completer abort received on the PCI Express interface
11	TABORT_SIG	RCU	Signaled target abort. This bit is set when the PCI Express interface completes a request with completer abort status. 0 = Completer abort not signaled on the PCI Express interface 1 = Completer abort signaled on the PCI Express interface
10:9	PCI_SPEED	R	DEVSEL timing. These bits are read-only 00b, because they do not apply to PCI Express.
8	DATAPAR	RCU	Master data parity error. This bit is set if bit 6 (PERR_ENB) in the command register (offset 04h, see Section 4.3) is set and the bridge receives a completion with data marked as poisoned on the PCI Express interface or poisons a write request received on the PCI Express interface. 0 = No uncorrectable data error detected on the primary interface 1 = Uncorrectable data error detected on the primary interface
7	FBB_CAP	R	Fast back-to-back capable. This bit does not have a meaningful context for a PCI Express device and is hardwired to 0b.
6	RSVD	R	Reserved. Returns 0b when read.
5	66MHZ	R	66-MHz capable. This bit does not have a meaningful context for a PCI Express device and is hardwired to 0b.
4	CAPLIST	R	Capabilities list. This bit returns 1b when read, indicating that the bridge supports additional PCI capabilities.
3	INT_STATUS	R	Interrupt status. This bit reflects the interrupt status of the function. This bit is read-only 0b since the bridge does not generate any interrupts internally.
2:0	RSVD	R	Reserved. Returns 000b when read.

Not Recommended for New Designs

4.5 Class Code and Revision ID Register

This read-only register categorizes the base class, subclass, and programming interface of the bridge. The base class is 06h, identifying the device as a bridge. The subclass is 04h, identifying the function as a PCI-to-PCI bridge, and the programming interface is 00h. Furthermore, the TI device revision is indicated in the lower byte (03h). See Table 4–4 for a complete description of the register contents.

PCI register offset: 08h
Register type: Read-only
Default value: 0604 0003

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0
BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Table 4–4. Class Code and Revision ID Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:24	BASECLASS	R	Base class. This field returns 06h when read, which classifies the function as a bridge device.
23:16	SUBCLASS	R	Subclass. This field returns 04h when read, which classifies the function as a PCI-to-PCI bridge.
15:8	PGMIF	R	Programming interface. This field returns 00h when read.
7:0	CHIPREV	R	Silicon revision. This field returns the silicon revision of the function.

4.6 Cache Line Size Register

This read/write cache line size register is used by the bridge to determine how much data to prefetch when handling delayed read transactions. The value in this register must be programmed to a power of 2. Any written odd value (bit 0 = 1b) or value greater than 32 DWORDs is treated as 0 DWORDs.

PCI register offset: 0Ch
Register type: Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.7 Primary Latency Timer Register

This read-only register has no meaningful context for a PCI Express device and returns 00h when read.

PCI register offset: 0Dh
Register type: Read-only
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.8 Header Type Register

This read-only register indicates that this function has a type one PCI header. Bit 7 of this register is 0b indicating that the bridge is a single-function device.

PCI register offset: 0Eh
Register type: Read-only
Default value: 01h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	1

Not Recommended for New Designs

4.9 BIST Register

Since the bridge does not support a built-in self test (BIST), this read-only register returns the value of 00h when read.

PCI register offset: 0Fh
Register type: Read-only
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.10 Device Control Base Address Register

This register programs the memory base address that accesses the device control registers. By default, this register is read only. If bit 5 of the Control and Diagnostic Register 2 (offset C8h) is set, then the bits 31:12 of this register become read/write. See Table 4–5 for a complete description of the register contents.

PCI register offset: 10h
Register type: Read-only, Read/Write
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4–5. Device Control Base Address Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:12	ADDRESS	R, RW	Memory base address. The memory address field for the bridge uses 20 read/write bits indicating that 4096 bytes is the amount of memory space that is reserved. These bits are read only if Register C8h bit 5 is clear. If bit 5 is set, then these bits become Read/Write.
11:4	RSVD	R	Reserved. These bits are read-only and return 00h when read.
3	PRE_FETCH	R	Prefetchable. This bit is read-only 0b indicating that this memory window is not prefetchable.
2:1	MEM_TYPE	R	Memory type. This field is read-only 00b indicating that this window can be located anywhere in the 32-bit address space.
0	MEM_IND	R	Memory space indicator. This field returns 0b indicating that memory space is used.

4.11 Primary Bus Number Register

This read/write register specifies the bus number of the PCI bus segment that the PCI Express interface is connected to.

PCI register offset: 18h
Register type: Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Not Recommended for New Designs

4.12 Secondary Bus Number Register

This read/write register specifies the bus number of the PCI bus segment that the PCI interface is connected to. The bridge uses this register to determine how to respond to a type 1 configuration transaction.

PCI register offset: 19h
Register type: Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.13 Subordinate Bus Number Register

This read/write register specifies the bus number of the highest number PCI bus segment that is downstream of the bridge. Since the PCI bus is internal and only connects to the 1394a OHCI, this register must always be equal to the secondary bus number register (offset 19h, see Section 4.12). The bridge uses this register to determine how to respond to a type 1 configuration transaction.

PCI register offset: 1Ah
Register type: Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.14 Secondary Latency Timer Register

This read/write register specifies the secondary bus latency timer for the bridge, in units of PCI clock cycles.

PCI register offset: 1Bh
Register type: Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.15 I/O Base Register

This read/write register specifies the lower limit of the I/O addresses that the bridge forwards downstream. See Table 4–6 for a complete description of the register contents.

PCI register offset: 1Ch
Register type: Read-only, Read/Write
Default value: 01h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	1

Table 4–6. I/O Base Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:4	IOBASE	RW	I/O base. Defines the bottom address of the I/O address range that determines when to forward I/O transactions from one interface to the other. These bits correspond to address bits [15:12] in the I/O address. The lower 12 bits are assumed to be 000h. The 16 bits corresponding to address bits [31:16] of the I/O address are defined in the I/O base upper 16 bits register (offset 30h, see Section 4.24).
3:0	IOTYPE	R	I/O type. This field is read-only 1h indicating that the bridge supports 32-bit I/O addressing.

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4.16 I/O Limit Register

This read/write register specifies the upper limit of the I/O addresses that the bridge forwards downstream. See Table 4–7 for a complete description of the register contents.

PCI register offset: 1Dh
Register type: Read-only, Read/Write
Default value: 01h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	1

Table 4–7. I/O Limit Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:4	IOLIMIT	RW	I/O limit. Defines the top address of the I/O address range that determines when to forward I/O transactions from one interface to the other. These bits correspond to address bits [15:12] in the I/O address. The lower 12 bits are assumed to be FFFh. The 16 bits corresponding to address bits [31:16] of the I/O address are defined in the I/O limit upper 16 bits register (offset 32h, see Section 4.25).
3:0	IOTYPE	R	I/O type. This field is read-only 1h indicating that the bridge supports 32-bit I/O addressing.

Not Recommended for New Designs

4.17 Secondary Status Register

The secondary status register provides information about the PCI bus interface. See Table 4–8 for a complete description of the register contents.

PCI register offset: 1Eh
Register type: Read-only, Read/Clear
Default value: 02X0h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	1	0	1	0	x	0	0	0	0	0

Table 4–8. Secondary Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15	PAR_ERR	RCU	Detected parity error. This bit reports the detection of an uncorrectable address, attribute, or data error by the bridge on its internal PCI bus secondary interface. This bit must be set when any of the following three conditions are true: • The bridge detects an uncorrectable address or attribute error as a potential target. • The bridge detects an uncorrectable data error when it is the target of a write transaction. • The bridge detects an uncorrectable data error when it is the master of a read transaction (immediate read data). The bit is set irrespective of the state of bit 0 (PERR_EN) in the bridge control register at offset 3Eh (see Section 4.29). 0 = Uncorrectable address, attribute, or data error not detected on secondary interface 1 = Uncorrectable address, attribute, or data error detected on secondary interface
14	SYS_ERR	RCU	Received system error. This bit is set when the bridge detects an $\overline{\text{SERR}}$ assertion. 0 = No error asserted on the PCI interface 1 = $\overline{\text{SERR}}$ asserted on the PCI interface
13	MABORT	RCU	Received master abort. This bit is set when the PCI interface of the bridge reports the detection of a master abort termination by the bridge when it is the master of a transaction on its secondary interface. 0 = Master abort not received on the PCI interface 1 = Master abort received on the PCI interface
12	TABORT_REC	RCU	Received target abort. This bit is set when the PCI interface of the bridge receives a target abort. 0 = Target abort not received on the PCI interface 1 = Target abort received on the PCI interface
11	TABORT_SIG	RCU	Signaled target abort. This bit reports the signaling of a target abort termination by the bridge when it responds as the target of a transaction on its secondary interface. 0 = Target abort not signaled on the PCI interface 1 = Target abort signaled on the PCI interface
10:9	PCI_SPEED	R	DEVSEL timing. These bits are 01b indicating that this is a medium speed decoding device.
8	DATAPAR	RCU	Master data parity error. This bit is set if the bridge is the bus master of the transaction on the PCI bus, bit 0 (PERR_EN) in the bridge control register (offset 3Eh see Section 4.29) is set, and the bridge either asserts $\overline{\text{PERR}}$ on a read transaction or detects $\overline{\text{PERR}}$ asserted on a write transaction. 0 = No data parity error detected on the PCI interface 1 = Data parity error detected on the PCI interface
7	FBB_CAP	R	Fast back-to-back capable. This bit returns a 1b when read indicating that the secondary PCI interface of bridge supports fast back-to-back transactions.
6	RSVD	R	Reserved. Returns 0b when read.
5	66MHZ	R	66-MHz capable. The bridge operates at a PCI bus CLK frequency of 66 MHz; therefore, this bit always returns a 1b.
4:0	RSVD	R	Reserved. Returns 00000b when read.

Not Recommended for New Designs

4.18 Memory Base Register

This read/write register specifies the lower limit of the memory addresses that the bridge forwards downstream. See Table 4–9 for a complete description of the register contents.

PCI register offset: 20h
Register type: Read-only, Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4–9. Memory Base Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	MEMBASE	RW	Memory base. Defines the lowest address of the memory address range that determines when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be 00000h.
3:0	RSVD	R	Reserved. Returns 0h when read.

4.19 Memory Limit Register

This read/write register specifies the upper limit of the memory addresses that the bridge forwards downstream. See Table 4–10 for a complete description of the register contents.

PCI register offset: 22h
Register type: Read-only, Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4–10. Memory Limit Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	MEMLIMIT	RW	Memory limit. Defines the highest address of the memory address range that determines when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be FFFFFh.
3:0	RSVD	R	Reserved. Returns 0h when read.

4.20 Prefetchable Memory Base Register

This read/write register specifies the lower limit of the prefetchable memory addresses that the bridge forwards downstream. See Table 4–11 for a complete description of the register contents.

PCI register offset: 24h
Register type: Read-only, Read/Write
Default value: 0001h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Table 4–11. Prefetchable Memory Base Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	PREBASE	RW	Prefetchable memory base. Defines the lowest address of the prefetchable memory address range that determines when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be 00000h. The prefetchable base upper 32 bits register (offset 28h, see Section 4.22) specifies the bit [63:32] of the 64-bit prefetchable memory address.
3:0	64BIT	R	64-bit memory indicator. These read-only bits indicate that 64-bit addressing is supported for this memory window.

Not Recommended for New Designs

4.21 Prefetchable Memory Limit Register

This read/write register specifies the upper limit of the prefetchable memory addresses that the bridge forwards downstream. See Table 4–12 for a complete description of the register contents.

PCI register offset: 26h
Register type: Read-only, Read/Write
Default value: 0001h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Table 4–12. Prefetchable Memory Limit Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	PRELIMIT	RW	Prefetchable memory limit. Defines the highest address of the prefetchable memory address range that determines when to forward memory transactions from one interface to the other. These bits correspond to address bits [31:20] in the memory address. The lower 20 bits are assumed to be FFFFFh. The prefetchable limit upper 32 bits register (offset 2Ch, see Section 4.23) specifies the bit [63:32] of the 64-bit prefetchable memory address.
3:0	64BIT	R	64-bit memory indicator. These read-only bits indicate that 64-bit addressing is supported for this memory window.

4.22 Prefetchable Base Upper 32 Bits Register

This read/write register specifies the upper 32 bits of the prefetchable memory base register. See Table 4–13 for a complete description of the register contents.

PCI register offset: 28h
Register type: Read/Write
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4–13. Prefetchable Base Upper 32 Bits Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:0	PREBASE	RW	Prefetchable memory base upper 32 bits. Defines the upper 32 bits of the lowest address of the prefetchable memory address range that determines when to forward memory transactions downstream.

4.23 Prefetchable Limit Upper 32 Bits Register

This read/write register specifies the upper 32 bits of the prefetchable memory limit register. See Table 4–14 for a complete description of the register contents.

PCI register offset: 2Ch
Register type: Read/Write
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4–14. Prefetchable Limit Upper 32 Bits Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:0	PRELIMIT	RW	Prefetchable memory limit upper 32 bits. Defines the upper 32 bits of the highest address of the prefetchable memory address range that determines when to forward memory transactions downstream.

Not Recommended for New Designs

4.24 I/O Base Upper 16 Bits Register

This read/write register specifies the upper 16 bits of the I/O base register. See Table 4–15 for a complete description of the register contents.

PCI register offset: 30h
Register type: Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4–15. I/O Base Upper 16 Bits Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:0	IOBASE	RW	I/O base upper 16 bits. Defines the upper 16 bits of the lowest address of the I/O address range that determines when to forward I/O transactions downstream. These bits correspond to address bits [31:20] in the I/O address. The lower 20 bits are assumed to be 00000h.

4.25 I/O Limit Upper 16 Bits Register

This read/write register specifies the upper 16 bits of the I/O limit register. See Table 4–16 for a complete description of the register contents.

PCI register offset: 32h
Register type: Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4–16. I/O Limit Upper 16 Bits Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:0	IOLIMIT	RW	I/O limit upper 16 bits. Defines the upper 16 bits of the top address of the I/O address range that determines when to forward I/O transactions downstream. These bits correspond to address bits [31:20] in the I/O address. The lower 20 bits are assumed to be FFFFFh.

4.26 Capabilities Pointer Register

This read-only register provides a pointer into the PCI configuration header where the PCI power management block resides. Since the PCI power management registers begin at 50h, this register is hardwired to 50h.

PCI register offset: 34h
Register type: Read-only
Default value: 50h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	1	0	1	0	0	0	0

Not Recommended for New Designs

4.27 Interrupt Line Register

This read/write register is programmed by the system and indicates to the software which interrupt line the bridge has assigned to it. The default value of this register is FFh, indicating that an interrupt line has not yet been assigned to the function. Since the bridge does not generate interrupts internally, this register is a scratch pad register.

PCI register offset: 3Ch
Register type: Read/Write
Default value: FFh

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	1	1	1	1	1	1	1	1

4.28 Interrupt Pin Register

The interrupt pin register is read-only 00h indicating that the bridge does not generate internal interrupts. While the bridge does not generate internal interrupts, it does forward interrupts from the secondary interface to the primary interface.

PCI register offset: 3Dh
Register type: Read-only
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.29 Bridge Control Register

The bridge control register provides extensions to the command register that are specific to a bridge. See Table 4–17 for a complete description of the register contents.

PCI register offset: 3Eh
Register type: Read-only, Read/Write, Read/Clear
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4–17. Bridge Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:12	RSVD	R	Reserved. Returns 0h when read.
11	DTSERR	RW	Discard timer $\overline{\text{SERR}}$ enable. Applies only in conventional PCI mode. This bit enables the bridge to generate either an ERR_NONFATAL (by default) or ERR_FATAL transaction on the primary interface when the secondary discard timer expires and a delayed transaction is discarded from a queue in the bridge. The severity is selectable only if advanced error reporting is supported. 0 = Do not generate ERR_NONFATAL or ERR_FATAL on the primary interface as a result of the expiration of the secondary discard timer. Note that an error message can still be sent if advanced error reporting is supported and bit 10 (DISCARD_TIMER_MASK) in the secondary uncorrectable error mask register (offset 130h, see Section 5.11) is clear (default). 1 = Generate ERR_NONFATAL or ERR_FATAL on the primary interface if the secondary discard timer expires and a delayed transaction is discarded from a queue in the bridge
10	DTSTATUS	RCU	Discard timer status. This bit indicates if a discard timer expires and a delayed transaction is discarded. 0 = No discard timer error 1 = Discard timer error

Not Recommended for New Designs

Table 4–17. Bridge Control Register Description (Continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
9	SEC_DT	RW	Selects the number of PCI clocks that the bridge waits for the 1394a OHCI master on the secondary interface to repeat a delayed transaction request. The counter starts once the delayed completion (the completion of the delayed transaction on the primary interface) has reached the head of the downstream queue of the bridge (i.e., all ordering requirements have been satisfied and the bridge is ready to complete the delayed transaction with the initiating master on the secondary bus). If the master does not repeat the transaction before the counter expires, then the bridge deletes the delayed transaction from its queue and sets the discard timer status bit. 0 = The secondary discard timer counts 2^{15} PCI clock cycles (default) 1 = The secondary discard timer counts 2^{10} PCI clock cycles
8	PRI_DEC	R	Primary discard timer. This bit has no meaning in PCI Express and is hardwired to 0b.
7	FBB_EN	RW	Fast back-to-back enable. This bit allows software to enable fast back-to-back transactions on the secondary PCI interface. 0 = Fast back-to-back transactions are disabled (default) 1 = Secondary interface fast back-to-back transactions are enabled
6	SRST	RW	Secondary bus reset. This bit is set when software wishes to reset all devices downstream of the bridge. Setting this bit causes the $\overline{\text{PRST}}$ signal on the secondary interface to be asserted. 0 = Secondary interface is not in reset state (default) 1 = Secondary interface is in the reset state
5	MAM	RW	Master abort mode. This bit controls the behavior of the bridge when it receives a master abort or an unsupported request. 0 = Do not report master aborts. Returns FFFF FFFFh on reads and discard data on writes (default) 1 = Respond with an unsupported request on PCI Express when a master abort is received on PCI. Respond with target abort on PCI when an unsupported request completion on PCI Express is received. This bit also enables error signaling on master abort conditions on posted writes.
4	VGA16	RW	VGA 16-bit decode. This bit enables the bridge to provide full 16-bit decoding for VGA I/O addresses. This bit only has meaning if the VGA enable bit is set. 0 = Ignore address bits [15:10] when decoding VGA I/O addresses (default) 1 = Decode address bits [15:10] when decoding VGA I/O addresses
3	VGA	RW	VGA enable. This bit modifies the response by the bridge to VGA compatible addresses. If this bit is set, then the bridge decodes and forwards the following accesses on the primary interface to the secondary interface (and, conversely, block the forwarding of these addresses from the secondary to primary interface): • Memory accesses in the range 000A 0000h to 000B FFFFh • I/O addresses in the first 64 KB of the I/O address space (address bits [31:16] are 0000h) and where address bits [9:0] are in the range of 3B0h to 3BBh or 3C0h to 3DFh (inclusive of ISA address aliases – address bits [15:10] may possess any value and are not used in the decoding) If this bit is set, then forwarding of VGA addresses is independent of the value of bit 2 (ISA), the I/O address and memory address ranges defined by the I/O base and limit registers, the memory base and limit registers, and the prefetchable memory base and limit registers of the bridge. The forwarding of VGA addresses is qualified by bits 0 (IO_ENB) and 1 (MEMORY_ENB) in the command register (offset 04h, see Section 4.3). 0 = Do not forward VGA compatible memory and I/O addresses from the primary to secondary interface (addresses defined above) unless they are enabled for forwarding by the defined I/O and memory address ranges (default) 1 = Forward VGA compatible memory and I/O addresses (addresses defined above) from the primary interface to the secondary interface (if the I/O enable and memory enable bits are set) independent of the I/O and memory address ranges and independent of the ISA enable bit

Not Recommended for New Designs

Table 4–17. Bridge Control Register Description (Continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
2	ISA	RW	ISA enable. This bit modifies the response by the bridge to ISA I/O addresses. This applies only to I/O addresses that are enabled by the I/O base and I/O limit registers and are in the first 64 KB of PCI I/O address space (0000 0000h to 0000 FFFFh). If this bit is set, then the bridge blocks any forwarding from primary to secondary of I/O transactions addressing the last 768 bytes in each 1-KB block. In the opposite direction (secondary to primary), I/O transactions are forwarded if they address the last 768 bytes in each 1K block. 0 = Forward downstream all I/O addresses in the address range defined by the I/O base and I/O limit registers (default) 1 = Forward upstream ISA I/O addresses in the address range defined by the I/O base and I/O limit registers that are in the first 64 KB of PCI I/O address space (top 768 bytes of each 1-KB block)
1	SERR_EN	RW	SERR enable. This bit controls forwarding of system error events from the secondary interface to the primary interface. The bridge forwards system error events when: • This bit is set • Bit 8 (SERR_ENB) in the command register (offset 04h, see Section 4.3) is set • $\overline{\text{SERR}}$ is asserted on the secondary interface 0 = Disable the forwarding of system error events (default) 1 = Enable the forwarding of system error events
0	PERR_EN	RW	Parity error response enable. Controls the bridge's response to data, uncorrectable address, and attribute errors on the secondary interface. Also, the bridge always forwards data with poisoning, from conventional PCI to PCI Express on an uncorrectable conventional PCI data error, regardless of the setting of this bit. 0 = Ignore uncorrectable address, attribute, and data errors on the secondary interface (default) 1 = Enable uncorrectable address, attribute, and data error detection and reporting on the secondary interface

4.30 Capability ID Register

This read-only register identifies the linked list item as the register for PCI power management. The register returns 01h when read.

PCI register offset: 50h
Register type: Read-only
Default value: 01h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	1

4.31 Next Item Pointer Register

The contents of this read-only register indicate the next item in the linked list of capabilities for the bridge. This register reads 60h pointing to the MSI capabilities registers.

PCI register offset: 51h
Register type: Read-only
Default value: 60h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	1	1	0	0	0	0	0

Not Recommended for New Designs

4.32 Power Management Capabilities Register

This read-only register indicates the capabilities of the bridge related to PCI power management. See Table 4–18 for a complete description of the register contents.

PCI register offset: 52h
Register type: Read-only
Default value: 0602h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1	0

Table 4–18. Power Management Capabilities Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:11	PME_SUPPORT	R	$\overline{PME}$ support. This 5-bit field indicates the power states from which the bridge may assert $\overline{PME}$. Because the bridge never generates a $\overline{PME}$ except on a behalf of a secondary device, this field is read-only and returns 00000b.
10	D2_SUPPORT	R	This bit returns a 1b when read, indicating that the function supports the D2 device power state.
9	D1_SUPPORT	R	This bit returns a 1b when read, indicating that the function supports the D1 device power state.
8:6	AUX_CURRENT	R	3.3 V_{AUX} auxiliary current requirements. This field returns 000b since the bridge does not generate $\overline{PME}$ from $D3_{cold}$.
5	DSI	R	Device specific initialization. This bit returns 0b when read, indicating that the bridge does not require special initialization beyond the standard PCI configuration header before a generic class driver is able to use it.
4	RSVD	R	Reserved. Returns 0b when read.
3	PME_CLK	R	$\overline{PME}$ clock. This bit returns 0b indicating that the PCI clock is not needed to generate $\overline{PME}$.
2:0	PM_VERSION	R	Power management version. If bit 26 (PCI_PM_VERSION_CTRL) in the general control register (offset D4h, see Section 4.65) is 0b, then this field returns 010b indicating revision 1.1 compatibility. If PCI_PM_VERSION_CTRL is 1b, then this field returns 011b indicating revision 1.2 compatibility.

Not Recommended for New Designs

4.33 Power Management Control/Status Register

This register determines and changes the current power state of the bridge. No internal reset is generated when transitioning from the $D3_{hot}$ state to the D0 state. See Table 4–19 for a complete description of the register contents.

PCI register offset: 54h
Register type: Read-only, Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4–19. Power Management Control/Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15	PME_STAT	R	$\overline{PME}$ status. This bit is read-only and returns 0b when read.
14:13	DATA_SCALE	R	Data scale. This 2-bit field returns 00b when read since the bridge does not use the data register.
12:9	DATA_SEL	R	Data select. This 4-bit field returns 0h when read since the bridge does not use the data register.
8	PME_EN	RW	$\overline{PME}$ enable. This bit has no function and acts as scratchpad space. The default value for this bit is 0b.
7:4	RSVD	R	Reserved. Returns 0h when read.
3	NO_SOFT_RESET	R	No soft reset. If bit 26 (PCI_PM_VERSION_CTRL) in the general control register (offset D4h, see Section 4.65) is 0b, then this bit returns 0b for compatibility with version 1.1 of the *PCI Power Management Specification*. If PCI_PM_VERSION_CTRL is 1b, then this bit returns 1b indicating that no internal reset is generated and the device retains its configuration context when transitioning from the $D3_{hot}$ state to the D0 state.
2	RSVD	R	Reserved. Returns 0b when read.
1:0	PWR_STATE	RW	Power state. This 2-bit field determines the current power state of the function and sets the function into a new power state. This field is encoded as follows: 00 = D0 (default) 01 = D1 10 = D2 11 = $D3_{hot}$

4.34 Power Management Bridge Support Extension Register

This read-only register indicates to host software what the state of the secondary bus will be when the bridge is placed in D3. See Table 4–20 for a complete description of the register contents.

PCI register offset: 56h
Register type: Read-only
Default value: 40h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	1	0	0	0	0	0	0

Table 4–20. PM Bridge Support Extension Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7	BPCC	R	Bus power/clock control enable. This bit indicates to the host software if the bus secondary clocks are stopped when the bridge is placed in D3. The state of the BPCC bit is controlled by bit 11 (BPCC_E) in the general control register (offset D4h, see Section 4.65). 0 = The secondary bus clocks are not stopped in D3 1 = The secondary bus clocks are stopped in D3
6	BSTATE	R	B2/B3 support. This bit is read-only 1b indicating that the bus state in D3 is B2.
5:0	RSVD	R	Reserved. Returns 00 0000b when read.

Not Recommended for New Designs

4.35 Power Management Data Register

The read-only register is not applicable to the bridge and returns 00h when read.

PCI register offset: 57h
Register type: Read-only
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.36 MSI Capability ID Register

This read-only register identifies the linked list item as the register for message signaled interrupts capabilities. The register returns 05h when read.

PCI register offset: 60h
Register type: Read-only
Default value: 05h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	1	0	1

4.37 Next Item Pointer Register

The contents of this read-only register indicate the next item in the linked list of capabilities for the bridge. This register reads 80h pointing to the subsystem ID capabilities registers.

PCI register offset: 61h
Register type: Read-only
Default value: 80h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	1	0	0	0	0	0	0	0

Not Recommended for New Designs

4.38 MSI Message Control Register

This register controls the sending of MSI messages. See Table 4–21 for a complete description of the register contents.

PCI register offset: 62h
Register type: Read-only, Read/Write
Default value: 0088h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0

Table 4–21. MSI Message Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:8	RSVD	R	Reserved. Returns 00h when read.
7	64CAP	R	64-bit message capability. This bit is read-only 1b indicating that the bridge supports 64-bit MSI message addressing.
6:4	MM_EN	RW	Multiple message enable. This bit indicates the number of distinct messages that the bridge is allowed to generate. 000 = 1 message (default) 001 = 2 messages 010 = 4 messages 011 = 8 messages 100 = 16 messages 101 = Reserved 110 = Reserved 111 = Reserved
3:1	MM_CAP	R	Multiple message capabilities. This field indicates the number of distinct messages that bridge is capable of generating. This field is read-only 100b indicating that the bridge can signal 1 interrupt for each IRQ supported on the serial IRQ stream up to a maximum of 16 unique interrupts.
0	MSI_EN	RW	MSI enable. This bit enables MSI interrupt signaling. MSI signaling must be enabled by software for the bridge to signal that a serial IRQ has been detected. 0 = MSI signaling is prohibited (default) 1 = MSI signaling is enabled

NOTE: Enabling MSI messaging in the XIO2200A has no effect.

4.39 MSI Message Lower Address Register

This register contains the lower 32 bits of the address that a MSI message writes to when a serial IRQ is detected. See Table 4–22 for a complete description of the register contents.

PCI register offset: 64h
Register type: Read-only, Read/Write
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4–22. MSI Message Lower Address Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:2	ADDRESS	RW	System specified message address
1:0	RSVD	R	Reserved. Returns 00b when read.

NOTE: Enabling MSI messaging in the XIO2200A has no effect.

Not Recommended for New Designs

4.40 MSI Message Upper Address Register

This register contains the upper 32 bits of the address that a MSI message writes to when a serial IRQ is detected. If this register contains 0000 0000h, then 32-bit addressing is used; otherwise, 64-bit addressing is used.

PCI register offset: 68h
Register type: Read/Write
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

NOTE: Enabling MSI messaging in the XIO2200A has no effect.

4.41 MSI Message Data Register

This register contains the data that software programmed the bridge to send when it send a MSI message. See Table 4–23 for a complete description of the register contents.

PCI register offset: 6Ch
Register type: Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4–23. MSI Message Data Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	MSG	RW	System specific message. This field contains the portion of the message that the bridge forwards unmodified.
3:0	MSG_NUM	RW	Message number. This portion of the message field may be modified to contain the message number is multiple messages are enable. The number of bits that are modifiable depends on the number of messages enabled in the message control register. 1 message = No message data bits can be modified (default) 2 messages = Bit 0 can be modified 4 messages = Bits 1:0 can be modified 8 messages = Bits 2:0 can be modified 16 messages = Bits 3:0 can be modified

NOTE: Enabling MSI messaging in the XIO2200A has no effect.

4.42 Capability ID Register

This read-only register identifies the linked list item as the register for subsystem ID and subsystem vendor ID capabilities. The register returns 0Dh when read.

PCI register offset: 80h
Register type: Read-only
Default value: 0Dh

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	1	1	0	1

Not Recommended for New Designs

4.43 Next Item Pointer Register

The contents of this read-only register indicate the next item in the linked list of capabilities for the bridge. This register reads 90h pointing to the PCI Express capabilities registers.

PCI register offset: 81h
Register type: Read-only
Default value: 90h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	1	0	0	1	0	0	0	0

4.44 Subsystem Vendor ID Register

This register, used for system and option card identification purposes, may be required for certain operating systems. This read-only register is initialized through the EEPROM and can be written through the subsystem alias register. This register is reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

PCI register offset: 84h
Register type: Read-only
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

4.45 Subsystem ID Register

This register, used for system and option card identification purposes, may be required for certain operating systems. This read-only register is initialized through the EEPROM and can be written through the subsystem alias register. This register is reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

PCI register offset: 86h
Register type: Read-only
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

4.46 PCI Express Capability ID Register

This read-only register identifies the linked list item as the register for PCI Express capabilities. The register returns 10h when read.

PCI register offset: 90h
Register type: Read-only
Default value: 10h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	1	0	0	0	0

Not Recommended for New Designs

4.47 Next Item Pointer Register

The contents of this read-only register indicate the next item in the linked list of capabilities for the bridge. This register reads 00h indicating no additional capabilities are supported.

PCI register offset: 91h
Register type: Read-only
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.48 PCI Express Capabilities Register

This read-only register indicates the capabilities of the bridge related to PCI Express. See Table 4–24 for a complete description of the register contents.

PCI register offset: 92h
Register type: Read-only
Default value: 0071h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1

Table 4–24. PCI Express Capabilities Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:9	RSVD	R	Reserved. Returns 000 0000b when read.
8	SLOT	R	Slot implemented. This bit is not valid for the bridge and is read-only 0b.
7:4	DEV_TYPE	R	Device/port type. This read-only field returns 0111b indicating that the device is a PCI Express-to-PCI bridge.
3:0	VERSION	R	Capability version. This field returns 1h indicating revision 1 of the PCI Express capability.

Not Recommended for New Designs

4.49 Device Capabilities Register

The device capabilities register indicates the device specific capabilities of the bridge. See Table 4–25 for a complete description of the register contents.

PCI register offset: 94h
Register type: Read-only
Default value: 0000 0D82

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	1	1	0	1	1	0	0	0	0	0	1	0

Table 4–25. Device Capabilities Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:28	RSVD	R	Reserved. Returns 0h when read.
27:26	CSPLS	RU	Captured slot power limit scale. The value in this field is programmed by the host by issuing a Set_Slot_Power_Limit message. When a Set_Slot_Power_Limit message is received, bits 9:8 are written to this field. The value in this field specifies the scale used for the slot power limit. 00 = 1.0x 01 = 0.1x 10 = 0.01x 11 = 0.001x
25:18	CSPLV	RU	Captured slot power limit value. The value in this field is programmed by the host by issuing a Set_Slot_Power_Limit message. When a Set_Slot_Power_Limit message is received, bits 7:0 are written to this field. The value in this field in combination with the slot power limit scale value (bits 27:26) specifies the upper limit of power supplied to the slot. The power limit is calculated by multiplying the value in this field by the value in the slot power limit scale field.
17:15	RSVD	R	Reserved. Return 000b when read.
14	PIP	R	Power indicator present. This bit is hardwired to 0b indicating that a power indicator is not implemented.
13	AIP	R	Attention indicator present. This bit is hardwired to 0b indicating that an attention indicator is not implemented.
12	ABP	R	Attention button present. This bit is hardwired to 0b indicating that an attention button is not implemented.
11:9	EP_L1_LAT	RU	Endpoint L1 acceptable latency. This field indicates the maximum acceptable latency for a transition from L1 to L0 state. This field can be programmed by writing to the L1_LATENCY field (bits 15:13) in the general control register (offset D4h, see Section 4.65). The default value for this field is 110b which indicates a range from 32 µs to 64 µs. This field cannot be programmed to be less than the latency for the PHY to exit the L1 state.
8:6	EP_L0S_LAT	RU	Endpoint L0s acceptable latency. This field indicates the maximum acceptable latency for a transition from L0s to L0 state. This field can be programmed by writing to the L0s_LATENCY field (bits 18:16) in the general control register (offset D4h, see Section 4.65). The default value for this field is 110b which indicates a range from 2 µs to 4 µs. This field cannot be programmed to be less than the latency for the PHY to exit the L0s state.
5	ETFS	R	Extended tag field supported. This field indicates the size of the tag field not supported.
4:3	PFS	R	Phantom functions supported. This field is read-only 00b indicating that function numbers are not used for phantom functions.
2:0	MPSS	R	Maximum payload size supported. This field indicates the maximum payload size that the device can support for TLPs. This field is encoded as 010b indicating the maximum payload size for a TLP is 512 bytes.

Not Recommended for New Designs

4.50 Device Control Register

The device control register controls PCI Express device specific parameters. See Table 4–26 for a complete description of the register contents.

PCI register offset: 98h
Register type: Read-only, Read/Write
Default value: 2800h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0

Table 4–26. Device Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15	CFG_RTRY_ENB	RW	Configuration retry status enable. When this read/write bit is set to 1b, the bridge returns a completion with completion retry status on PCI Express if a configuration transaction forwarded to the secondary interface did not complete within the implementation specific time-out period. When this bit is set to 0b, the bridge does not generate completions with completion retry status on behalf of configuration transactions. The default value of this bit is 0b.
14:12	MRRS	RW	Maximum read request size. This field is programmed by host software to set the maximum size of a read request that the bridge can generate. The bridge uses this field in conjunction with the cache line size register (offset 0Ch, see Section 4.6) to determine how much data to fetch on a read request. This field is encoded as: 000 = 128B 001 = 256B 010 = 512B (default) 011 = 1024B 100 = 2048B 101 = 4096B 110 = Reserved 111 = Reserved
11	ENS	RW	Enable no snoop. Controls the setting of the no snoop flag within the TLP header for upstream memory transactions mapped to any traffic class mapped to a virtual channel (VC) other than VC0 through the upstream decode windows. 0 = No snoop field is 0b 1 = No snoop field is 1b (default)
10☆	APPE	RW	Auxiliary power PM enable. This bit has no effect in the bridge. 0 = AUX power is disabled (default) 1 = AUX power is enabled
9	PFE	R	Phantom function enable. Since the bridge does not support phantom functions, this bit is read-only 0b.
8	ETFE	R	Extended tag field enable. Since the bridge does not support extended tags, this bit is read-only 0b.
7:5	MPS	RW	Maximum payload size. This field is programmed by host software to set the maximum size of posted writes or read completions that the bridge can initiate. This field is encoded as: 000 = 128B (default) 001 = 256B 010 = 512B 011 = 1024B 100 = 2048B 101 = 4096B 110 = Reserved 111 = Reserved
4	ERO	R	Enable relaxed ordering. Since the bridge does not support relaxed ordering, this bit is read-only 0b.

☆This bit is sticky and must retain its value when the bridge is powered by V_{AUX}.

Not Recommended for New Designs

Table 4–26. Device Control Register Description (Continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
3	URRE	RW	Unsupported request reporting enable. If this bit is set, then the bridge sends an ERR_NONFATAL message to the root complex when an unsupported request is received. 0 = Do not report unsupported requests to the root complex (default) 1 = Report unsupported requests to the root complex
2	FERE	RW	Fatal error reporting enable. If this bit is set, then the bridge is enabled to send ERR_FATAL messages to the root complex when a system error event occurs. 0 = Do not report fatal errors to the root complex (default) 1 = Report fatal errors to the root complex
1	NFERE	RW	Nonfatal error reporting enable. If this bit is set, then the bridge is enabled to send ERR_NONFATAL messages to the root complex when a system error event occurs. 0 = Do not report nonfatal errors to the root complex (default) 1 = Report nonfatal errors to the root complex
0	CERE	RW	Correctable error reporting enable. If this bit is set, then the bridge is enabled to send ERR_COR messages to the root complex when a system error event occurs. 0 = Do not report correctable errors to the root complex (default) 1 = Report correctable errors to the root complex.

4.51 Device Status Register

The device status register provides PCI Express device specific information to the system. See Table 4–27 for a complete description of the register contents.

PCI register offset: 9Ah
Register type: Read-only
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4–27. Device Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:6	RSVD	R	Reserved. Returns 00 0000 0000b when read.
5	PEND	RU	Transaction pending. This bit is set when the bridge has issued a nonposted transaction that has not been completed.
4	APD	RU	AUX power detected. This bit indicates that AUX power is present. 0 = No AUX power detected 1 = AUX power detected
3	URD	RCU	Unsupported request detected. This bit is set by the bridge when an unsupported request is received.
2	FED	RCU	Fatal error detected. This bit is set by the bridge when a fatal error is detected.
1	NFED	RCU	Nonfatal error detected. This bit is set by the bridge when a nonfatal error is detected.
0	CED	RCU	Correctable error detected. This bit is set by the bridge when a correctable error is detected.

Not Recommended for New Designs

4.52 Link Capabilities Register

The link capabilities register indicates the link specific capabilities of the bridge. See Table 4–28 for a complete description of the register contents.

PCI register offset: 9Ch
Register type: Read-only
Default value: 0002 XC11h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	x	x	x	x	1	1	0	0	0	0	0	1	0	0	0	1

Table 4–28. Link Capabilities Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:24	PORT_NUM	R	Port number. This field indicates port number for the PCI Express link. This field is read-only 00h indicating that the link is associated with port 0.
23:18	RSVD	R	Reserved. Return 00 0000b when read.
17:15	L1_LATENCY	R	L1 exit latency. This field indicates the time that it takes to transition from the L1 state to the L0 state. Bit 6 (CCC) in the link control register (offset A0h, see Section 4.53) equals 1b for a common clock and equals 0b for an asynchronous clock. For a common reference clock, the value of this field is determined by bits 20:18 (L1_EXIT_LAT_ASYNC) of the control and diagnostic register 1 (offset C4h, see Section 4.62). For an asynchronous reference clock, the value of this field is determined by bits 17:15 (L1_EXIT_LAT_COMMON) of the control and diagnostic register 1 (offset C4h, see Section 4.62).
14:12	L0S_LATENCY	R	L0s exit latency. This field indicates the time that it takes to transition from the L0s state to the L0 state. Bit 6 (CCC) in the link control register (offset A0h, see Section 4.53) equals 1b for a common clock and equals 0b for an asynchronous clock. For a common reference clock, the value of 011b indicates that the L1 exit latency falls between 256 ns to less than 512 ns. For an asynchronous reference clock, the value of 100b indicates that the L1 exit latency falls between 512 ns to less than 1 µs.
11:10	ASLPMS	R	Active state link PM support. This field indicates the level of active state power management that the bridge supports. The value 11b indicates support for both L0s and L1 through active state power management.
9:4	MLW	R	Maximum link width. This field is encoded 00 0001b to indicate that the bridge only supports a 1x PCI Express link.
3:0	MLS	R	Maximum link speed. This field is encoded 1h to indicate that the bridge supports a maximum link speed of 2.5 Gb/s.

Not Recommended for New Designs

4.53 Link Control Register

The link control register controls link specific behavior. See Table 4–29 for a complete description of the register contents.

PCI register offset: A0h
Register type: Read-only, Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4–29. Link Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:8	RSVD	RW	Reserved. Returns 00h when read.
7	ES	RW	Extended synch. This bit forces the bridge to extend the transmission of FTS ordered sets and an extra TS2 when exiting from L1 prior to entering to L0. 0 = Normal synch (default) 1 = Extended synch
6	CCC	RW	Common clock configuration. When this bit is set, it indicates that the bridge and the device at the opposite end of the link are operating with a common clock source. A value of 0b indicates that the bridge and the device at the opposite end of the link are operating with separate reference clock sources. The bridge uses this common clock configuration information to report the correct L0s and L1 exit latencies. 0 = Reference clock is asynchronous (default) 1 = Reference clock is common
5	RL	R	Retrain link. This bit has no function and is read-only 0b.
4	LD	R	Link disable. This bit has no function and is read-only 0b.
3	RCB	RW	Read completion boundary. This bit is an indication of the RCB of the root complex. The state of this bit has no affect on the bridge, since the RCB of the bridge is fixed at 128 bytes. 0 = 64 bytes (default) 1 = 128 bytes
2	RSVD	R	Reserved. Returns 0b when read.
1:0	ASLPMC	RW	Active state link PM control. This field enables and disables the active state PM. 00 = Active state PM disabled (default) 01 = L0s entry enabled 10 = L1 entry enabled 11 = L0s and L1 entry enabled

Not Recommended for New Designs

4.54 Link Status Register

The link status register indicates the current state of the PCI Express link. See Table 4–30 for a complete description of the register contents.

PCI register offset: A2h
Register type: Read-only
Default value: X011h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	x	0	0	0	0	0	0	0	1	0	0	0	1

Table 4–30. Link Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:13	RSVD	R	Reserved. Returns 000b when read.
12	SCC	R	Slot clock configuration. This bit indicates that the bridge uses the same physical reference clock that the platform provides on the connector. If the bridge uses an independent clock irrespective of the presence of a reference on the connector, then this bit must be cleared. 0 = Independent 125-MHz reference clock is used 1 = Common 100-MHz reference clock is used
11	LT	R	Link training. This bit has no function and is read-only 0b.
10	TE	R	Retrain link. This bit has no function and is read-only 0b.
9:4	NLW	R	Negotiated link width. This field is read-only 00 0001b indicating the lane width is 1x.
3:0	LS	R	Link speed. This field is read-only 1h indicating the link speed is 2.5 Gb/s.

4.55 Serial-Bus Data Register

The serial-bus data register reads and writes data on the serial-bus interface. Write data is loaded into this register prior to writing the serial-bus slave address register (offset B2h, see Section 4.57) that initiates the bus cycle. When reading data from the serial bus, this register contains the data read after bit 5 (REQBUSY) of the serial-bus control and status register (offset B3h, see Section 4.58) is cleared. This register is reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

PCI register offset: B0h
Register type: Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.56 Serial-Bus Word Address Register

The value written to the serial-bus word address register represents the word address of the byte being read from or written to the serial-bus device. The word address is loaded into this register prior to writing the serial-bus slave address register (offset B2h, see Section 4.57) that initiates the bus cycle. This register is reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

PCI register offset: B1h
Register type: Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Not Recommended for New Designs

4.57 Serial-Bus Slave Address Register

The serial-bus slave address register indicates the slave address of the device being targeted by the serial-bus cycle. This register also indicates if the cycle is a read or a write cycle. Writing to this register initiates the cycle on the serial interface. See Table 4–31 for a complete description of the register contents.

PCI register offset: B2h
Register type: Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 4–31. Serial-Bus Slave Address Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:1†	SLAVE_ADDR	RW	Serial-bus slave address. This 7-bit field is the slave address for a serial-bus read or write transaction. The default value for this field is 000 0000b.
0†	RW_CMD	RW	Read/write command. This bit determines if the serial-bus cycle is a read or a write cycle. 0 = A single byte write is requested (default). 1 = A single byte read is requested.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Not Recommended for New Designs

4.58 Serial-Bus Control and Status Register

The serial-bus control and status register controls the behavior of the serial-bus interface. This register also provides status information about the state of the serial bus. See Table 4–32 for a complete description of the register contents.

PCI register offset: B3h
Register type: Read-only, Read/Write, Read/Clear
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 4–32. Serial-Bus Control and Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7†	PROT_SEL	RW	Protocol select. This bit selects the serial-bus address mode used. 0 = Slave address and word address are sent on the serial-bus (default) 1 = Only the slave address is sent on the serial-bus
6	RSVD	R	Reserved. Returns 0b when read.
5†	REQBUSY	RU	Requested serial-bus access busy. This bit is set when a software-initiated serial-bus cycle is in progress. 0 = No serial-bus cycle 1 = Serial-bus cycle in progress
4†	ROMBUSY	RU	Serial EEPROM access busy. This bit is set when the serial EEPROM circuitry in the bridge is downloading register defaults from a serial EEPROM. 0 = No EEPROM activity 1 = EEPROM download in progress
3†	SBDETECT	RWU	Serial EEPROM detected. This bit enables the serial-bus interface. The value of this bit controls whether the GPIO4//SCL and GPIO5//SDA terminals are configured as GPIO signals or as serial-bus signals. This bit is automatically set to 1b when a serial EEPROM is detected. **Note:** A serial EEPROM is only detected once following $\overline{\text{PERST}}$. 0 = No EEPROM present, EEPROM load process does not happen. GPIO4//SCL and GPIO5//SDA terminals are configured as GPIO signals. 1 = EEPROM present, EEPROM load process takes place. GPIO4//SCL and GPIO5//SDA terminals are configured as serial-bus signals.
2†	SBTEST	RW	Serial-bus test. This bit is used for internal test purposes. This bit controls the clock source for the serial interface clock. 0 = Serial-bus clock at normal operating frequency ~ 60 kHz (default) 1 = Serial-bus clock frequency increased for test purposes ~ 4 MHz
1†	SB_ERR	RCU	Serial-bus error. This bit is set when an error occurs during a software-initiated serial-bus cycle. 0 = No error 1 = Serial-bus error
0†	ROM_ERR	RCU	Serial EEPROM load error. This bit is set when an error occurs while downloading registers from a serial EEPROM. 0 = No error 1 = EEPROM load error

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Not Recommended for New Designs

4.59 GPIO Control Register

This register controls the direction of the eight GPIO terminals. This register has no effect on the behavior of GPIO terminals that are enabled to perform secondary functions. The secondary functions share GPIO4 (SCL) and GPIO5 (SDA). See Table 4–33 for a complete description of the register contents.

PCI register offset: B4h
Register type: Read-only, Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4–33. GPIO Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:8	RSVD	R	Reserved. Return 00h when read.
7†	GPIO7_DIR	RW	GPIO 7 data direction. This bit selects whether GPIO7 is in input or output mode. 0 = Input (default) 1 = Output
6†	GPIO6_DIR	RW	GPIO 6 data direction. This bit selects whether GPIO6 is in input or output mode. 0 = Input (default) 1 = Output
5†	GPIO5_DIR	RW	GPIO 5 data direction. This bit selects whether GPIO5 is in input or output mode. 0 = Input (default) 1 = Output
4†	GPIO4_DIR	RW	GPIO 4 data direction. This bit selects whether GPIO4 is in input or output mode. 0 = Input (default) 1 = Output
3†	GPIO3_DIR	RW	GPIO 3 data direction. This bit selects whether GPIO3 is in input or output mode. 0 = Input (default) 1 = Output
2†	GPIO2_DIR	RW	GPIO 2 data direction. This bit selects whether GPIO2 is in input or output mode. 0 = Input (default) 1 = Output
1†	GPIO1_DIR	RW	GPIO 1 data direction. This bit selects whether GPIO1 is in input or output mode. 0 = Input (default) 1 = Output
0†	GPIO0_DIR	RW	GPIO 0 data direction. This bit selects whether GPIO0 is in input or output mode. 0 = Input (default) 1 = Output

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Not Recommended for New Designs

4.60 GPIO Data Register

This register reads the state of the input mode GPIO terminals and changes the state of the output mode GPIO terminals. Writing to a bit that is in input mode or is enabled for a secondary function is ignored. The secondary functions share GPIO4 (SCL) and GPIO5 (SDA). The default value at power up depends on the state of the GPIO terminals as they default to general-purpose inputs. See Table 4–34 for a complete description of the register contents.

PCI register offset: B6h
Register type: Read-only, Read/Write
Default value: 00XXh

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

Table 4–34. GPIO Data Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:8	RSVD	R	Reserved
7†	GPIO7_DATA	RW	GPIO 7 data. This bit reads the state of GPIO7 when in input mode or changes the state of GPIO7 when in output mode.
6†	GPIO6_DATA	RW	GPIO 6 data. This bit reads the state of GPIO6 when in input mode or changes the state of GPIO6 when in output mode.
5†	GPIO5_DATA	RW	GPIO 5 data. This bit reads the state of GPIO5 when in input mode or changes the state of GPIO5 when in output mode.
4†	GPIO4_DATA	RW	GPIO 4 data. This bit reads the state of GPIO4 when in input mode or changes the state of GPIO4 when in output mode.
3†	GPIO3_DATA	RW	GPIO 3 data. This bit reads the state of GPIO3 when in input mode or changes the state of GPIO3 when in output mode.
2†	GPIO2_DATA	RW	GPIO 2 data. This bit reads the state of GPIO2 when in input mode or changes the state of GPIO2 when in output mode.
1†	GPIO1_DATA	RW	GPIO 1 data. This bit reads the state of GPIO1 when in input mode or changes the state of GPIO1 when in output mode.
0†	GPIO0_DATA	RW	GPIO 0 data. This bit reads the state of GPIO0 when in input mode or changes the state of GPIO0 when in output mode.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Not Recommended for New Designs

4.61 Control and Diagnostic Register 0

The contents of this register are used for monitoring status and controlling behavior of the bridge. See Table 4–35 for a complete description of the register contents. It is recommended that all values within this register be left at the default value. Improperly programming fields in this register may cause interoperability or other problems.

PCI register offset: C0h
Register type: Read/Write
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4–35. Control and Diagnostic Register 0 Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:24†	PRI_BUS_NUM	R	This field contains the captured primary bus number
23:19†	PRI_DEVICE_ NUM	R	This field contains the captured primary device number
18:16	RSVD	R	Reserved. Returns 000b when read.
15:14†	RSVD	RW	Reserved. Bits 15:14 default to 00b. If this register is programmed via EEPROM or another mechanism, the value written into this field must be 00b.
13:12	RSVD	R	Reserved. Returns 00b when read.
11:8†	RSVD	RW	Reserved. Bits 11:8 default to 0000b. If this register is programmed via EEPROM or another mechanism, the value written into this field must be 0000b.
7	RSVD	R	Reserved. Returns 0b when read.
6†	PREFETCH_4X	RW	Prefetch 4X enable. This bit sets the prefetch behavior for upstream memory read multiple transactions. If bit 24 (FORCE_MRM) in the general control register (offset D4h, see Section 4.65) is set, then all upstream memory read transactions will prefetch the indicated number of cache lines. If bit 19 (READ_PREFETCH_DIS) in the general control register (offset D4h, see Section 4.65) is set, then this bit has no effect and only 1 DWORD will be fetched. 0 = The bridge will prefetch up to 2 cache lines, as defined in the cache line size register (offset 0Ch, see Section 4.6) for upstream memory read multiple (MRM) transactions (default) 1 = The bridge device will prefetch up to 4 cache lines, as defined in the cache line size register (offset 0Ch, see Section 4.6) for upstream memory read multiple (MRM) transactions.
5:4†	UP_REQ_BUF _VALUE	RW	PCI upstream req-res buffer threshold value. The value in this field controls the buffer space that must be available for the bridge to accept a PCI bus transaction. If the cache line size is not valid, then the bridge will use 8 DW for calculating the threshold value 00 = 1 Cacheline + 4 DW (default) 01 = 1 Cacheline + 8 DW 10 = 1 Cacheline + 12 DW 11 = 2 Cachelines + 4 DW
3†	UP_REQ_BUF _CTRL	RW	PCI upstream req-res buffer threshold control. This bit enables the PCI upstream req-res buffer threshold control mode of the bridge. 0 = PCI upstream req-res buffer threshold control mode disabled (default) 1 = PCI upstream req-res buffer threshold control mode enabled
2†	CFG_ACCESS _MEM_REG	RW	Configuration access to memory-mapped registers. When this bit is set, the bridge allows configuration access to memory-mapped configuration registers.
1†	RSVD	RW	Reserved. Bit 1 defaults to 0b. If this register is programmed via EEPROM or another mechanism, the value written into this field must be 0b.
0	RSVD	R	Reserved. Returns 0b when read.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Not Recommended for New Designs

4.62 Control and Diagnostic Register 1

The contents of this register are used for monitoring status and controlling behavior of the bridge. See Table 4–36 for a complete description of the register contents. It is recommended that all values within this register be left at the default value. Improperly programming fields in this register may cause interoperability or other problems.

PCI register offset: C4h
Register type: Read/Write
Default value: 0012 0108h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0

Table 4–36. Control and Diagnostic Register 1 Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
32:21	RSVD	R	Reserved. Returns 000h when read.
20:18†	L1_EXIT_LAT_ ASYNC	RW	L1 exit latency for asynchronous clock. When bit 6 (CCC) of the link control register (offset A0h, see Section 4.53) is set, the value in this field is mirrored in bits 17:15 (L1_LATENCY) field in the link capabilities register (offset 9Ch, see Section 4.52). This field defaults to 100b.
17:15†	L1_EXIT_LAT_ COMMON	RW	L1 exit latency for common clock. When bit 6 (CCC) of the link control register (offset A0h, see Section 4.53) is clear, the value in this field is mirrored in bits 17:15 (L1_LATENCY) field in the link capabilities register (offset 9Ch, see Section 4.52). This field defaults to 100b.
14:11†	RSVD	RW	Reserved. Bits 14:11 default to 0000b. If this register is programmed via EEPROM or another mechanism, the value written into this field must be 0000b.
10†	SBUS_RESET _MASK	RW	Secondary bus reset bit mask. When this bit is set, the bridge masks the reset caused by bit 6 (SRST) of the bridge control register (offset 3Eh, see Section 4.29). This bit defaults to 0b.
9:6†	L1ASPM_ TIMER	RW	L1ASPM entry timer. This field specifies the value (in 512-ns ticks) of the L1ASPM entry timer. This field defaults to 0100b.
5:2†	L0s_TIMER	RW	L0s entry timer. This field specifies the value (in 62.5-MHz clock ticks) of the L0s entry timer. This field defaults to 0010b.
1:0†	RSVD	RW	Reserved. Bits 1:0 default to 00b. If this register is programmed via EEPROM or another mechanism, then the value written into this field must be 00b.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Not Recommended for New Designs

4.63 Control and Diagnostic Register 2

The contents of this register are used for monitoring status and controlling behavior of the bridge. See Table 4–37 for a complete description of the register contents. It is recommended that all values within this register be left at the default value. Improperly programming fields in this register may cause interoperability or other problems.

PCI register offset: C8h
Register type: Read/Write
Default value: 3214 6000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	1	1	0	0	1	0	0	0	0	1	0	1	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4–37. Control and Diagnostic Register 2 Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:24†	N_FTS_ ASYNC_CLK	RW	N_FTS for asynchronous clock. When bit 6 (CCC) of the link control register (offset A0h, see Section 4.53) is clear, the value in this field is the number of FTS that are sent on a transition from L0s to L0. This field shall default to 32h.
23:16†	N_FTS_ COMMON_ CLK	RW	N_FTS for common clock. When bit 6 (CCC) of the link control register (offset A0h, see Section 4.53) is set, the value in this field is the number of FTS that are sent on a transition from L0s to L0. This field defaults to 14h.
15:13	PHY_REV	R	PHY revision number
12:8†	LINK_NUM	RW	Link number
7:6	RSVD	R	Reserved. Returns 00b when read.
5:0	BAROWE	RW	BAR 0 Write Enable. When this bit is clear (default), the the Base Address Register at offset 10h is read only and writes to that register will have no effect. When this bit is set , then the bits 32:12 of the Base Address Register becomes writeable allowing the address of the 4K window to the Memory Mapped TI Proprietary Registers to be changed.
4:0†	RSVD	RW	Reserved. Bits 4:0 default to 00000b. If this register is programmed via EEPROM or another mechanism, then the value written into this field must be 00000b.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

4.64 Subsystem Access Register

The contents of this read/write register are aliased to the subsystem vendor ID and subsystem ID registers at PCI offsets 84h and 86h. See Table 4–38 for a complete description of the register contents.

PCI register offset: D0h
Register type: Read/Write
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4–38. Subsystem Access Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:16†	SubsystemID	RW	Subsystem ID. The value written to this field is aliased to the subsystem ID register at PCI offset 86h (see Section 4.45).
15:0†	SubsystemVendorID	RW	Subsystem vendor ID. The value written to this field is aliased to the subsystem vendor ID register at PCI offset 84h (see Section 4.44).

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Not Recommended for New Designs

4.65 General Control Register

This read/write register controls various functions of the bridge. See Table 4–39 for a complete description of the register contents.

PCI register offset: D4h
Register type: Read-only, Read/Write
Default value: 8206 C000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	1	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4–39. General Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:30†	CFG_RETRY _CNTR	RW	Configuration retry counter. Configures the amount of time that a configuration request must be retried on the secondary PCI bus before it may be completed with configuration retry status on the PCI Express side. 00 = 25 µs 01 = 1 ms 10 = 25 ms (default) 11 = 50 ms
29:28	RSVD	R	Reserved. Returns 00b when read.
27†	LOW_POWER _EN	RW	Low-power enable. When this bit is set, the half-ampitude, no preemphasis mode for the PCI Express TX drivers is enabled. The default for this bit is 0b.
26†	PCI_PM_ VERSION_ CTRL	RW	PCI power management version control. This bit controls the value reported in bits 2:0 (PM_VERSION) in the power management capabilities register (offset 52h, see Section 4.32). It also controls the value of bit 3 (NO_SOFT_RESET) in the power management control/status register (offset 54h, see Section 4.33). 0 = Version fields reports 010b and NO_SOFT_RESET reports 0b for Power Management 1.1 compliance (default) 1 = Version fields reports 011b and NO_SOFT_RESET reports 1b for Power Management 1.2 compliance
25†	STRICT_ PRIORITY_EN	RW	Strict priority enable. When this bit is set and bits 6:4 (LOW_PRIORITY_COUNT) in the port VC capability register 1 (offset 154h, see Section 5.17) are 000b, meaning that strict priority VC arbitration is used, the extended VC always receives priority over VC0 at the PCI Express port. 0 = The default LOW_PRIORITY_COUNT is 001b 1 = The default LOW_PRIORITY_COUNT is 000b (default)
24†	FORCE_MRM	RW	Force memory read multiple 0 = Memory read multiple transactions are disabled (default) 1 = All upstream memory read transactions initiated on the PCI bus are treated as though they are memory read multiple transactions where prefetching is supported
23†	ASPM_CTRL_ DEF_OVRD	RW	Active state power management control default override. This bit determines the power-up default for bits 1:0 (ASLPMC) of the link control register (offset A0h, see Section 4.53) in the PCI Express capability structure. 0 = Power-on default indicates that active state power management is disabled (00b) (default) 1 = Power-on default indicates that active state power management is enabled for L0s and L1 (11b)
22:20†	POWER_ OVRD	RW	Power override. This bit field determines how the bridge responds when the slot power limit is less than the amount of power required by the bridge and the devices behind the bridge. 000 = Ignore slot power limit (default). 001 = Assert the PWR_OVRD terminal. 010 = Disable secondary clocks selected by the clock mask register. 011 = Disable secondary clocks selected by the clock mask register and assert the PWR_OVRD terminal. 100 = Respond with unsupported request to all transactions except for configuration transactions (type 0 or type 1) and set slot power limit messages. 101, 110, 111 = Reserved

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Not Recommended for New Designs

Table 4–39. General Control Register Description (Continued)

BIT	FIELD NAME	ACCESS	DESCRIPTION
19†	READ_ PREFETCH_ DIS	RW	Read prefetch disable. This bit controls the prefetch functionality on PCI memory read transactions. 0 = Prefetch to the next cache line boundary on a burst read (default) 1 = Fetch only a single DWORD on a burst read
18:16†	L0s_LATENCY	RW	L0s maximum exit latency. This field programs the maximum acceptable latency when exiting the L0s state. This sets bits 8:6 (EP_L0S_LAT) in the device capabilities register (offset 94h, see Section 4.49). 000 = Less than 64 ns 001 = 64 ns up to less than 128 ns 010 = 128 ns up to less than 256 ns 011 = 256 ns up to less than 512 ns 100 = 512 ns up to less than 1 µs 101 = 1 µs up to less than 2 µs 110 = 2 µs to 4 µs (default) 111 = More than 4 µs
15:13†	L1_LATENCY	RW	L1 maximum exit latency. This field programs the maximum acceptable latency when exiting the L1 state. This sets bits 11:9 (EP_L1_LAT) in the device capabilities register (offset 94h, see Section 4.49). 000 = Less than 1 µs 001 = 1 µs up to less than 2 µs 010 = 2 µs up to less than 4 µs 011 = 4 µs up to less than 8 µs 100 = 8 µs up to less than 16 µs 101 = 16 µs up to less than 32 µs 110 = 32 µs to 64 µs (default) 111 = More than 64 µs
12†	VC_CAP_EN	RW	VC capability structure enable. This bit enables the VC capability structure by changing the next offset field of the advanced error reporting capability register at offset 102h. 0 = VC capability structure disabled (offset field = 000h) 1 = VC capability structure enabled (offset field = 150h)
11☆	BPCC_E	RW	Bus power clock control enable. This bit controls whether the secondary bus PCI clocks are stopped when the bridge is placed in the D3 state. It is assumed that if the secondary bus clocks are required to be active, that a reference clock continues to be provided on the PCI Express interface. 0 = Secondary bus clocks are not stopped in D3 (default) 1 = Secondary bus clocks are stopped on D3
10☆	BEACON_ ENABLE	RW	Beacon enable. This bit controls the mechanism for waking up the physical PCI Express link when in L2. 0 = $\overline{\text{WAKE}}$ mechanism is used exclusively. Beacon is not used (default) 1 = Beacon and $\overline{\text{WAKE}}$ mechanisms are used
9:8†	MIN_POWER_ SCALE	RW	Minimum power scale. This value is programmed to indicate the scale of bits 7:0 (MIN_POWER_VALUE). 00 = 1.0x (default) 01 = 0.1x 10 = 0.01x 11 = 0.001x
7:0†	MIN_POWER_ VALUE	RW	Minimum power value. This value is programmed to indicate the minimum power requirements. This value is multiplied by the minimum power scale field (bits 9:8) to determine the minimum power requirements for the bridge. The default is 00h, because this feature is only usable when the system implementer adds the PCI devices' power consumption to the bridge power consumption and reprograms this field with an EEPROM or the system BIOS.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

☆These bits are sticky and must retain their value when the bridge is powered by V_{AUX}.

Not Recommended for New Designs

4.66 TI Proprietary Register

This read/write TI proprietary register is located at offset D8h and controls TI proprietary functions. This register must not be changed from the specified default state. This register is reset by a PCI Express reset ($\overline{PERST}$), a $\overline{GRST}$, or the internally-generated power-on reset.

PCI register offset: D8h
Register type: Read-only, Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.67 TI Proprietary Register

This read/write TI proprietary register is located at offset D9h and controls TI proprietary functions. This register must not be changed from the specified default state. This register is reset by a PCI Express reset ($\overline{PERST}$), a $\overline{GRST}$, or the internally-generated power-on reset.

PCI register offset: D9h
Register type: Read-only, Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.68 TI Proprietary Register

This read-only TI proprietary register is located at offset DAh and controls TI proprietary functions. This register must not be changed from the specified default state. This register is reset by a PCI Express reset ($\overline{PERST}$), a $\overline{GRST}$, or the internally-generated power-on reset.

PCI register offset: DAh
Register type: Read-only
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Not Recommended for New Designs

4.69 Arbiter Control Register

The arbiter control register controls the bridge internal arbiter. The arbitration scheme used is a two-tier rotational arbitration. The bridge is the only secondary bus master that defaults to the higher priority arbitration tier. See Table 4–40 for a complete description of the register contents.

PCI register offset: DCh
Register type: Read/Write
Default value: 40h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	1	0	0	0	0	0	0

Table 4–40. Arbiter Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7†	PARK	RW	Bus parking mode. This bit determines where the internal arbiter parks the secondary bus. When this bit is set, the arbiter parks the secondary bus on the bridge. When this bit is cleared, the arbiter parks the bus on the last device mastering the secondary bus. 0 = Park the secondary bus on the last secondary bus master (default) 1 = Park the secondary bus on the bridge
6†	BRIDGE_TIER_SEL	RW	Bridge tier select. This bit determines in which tier the bridge is placed in the arbitration scheme. 0 = Lowest priority tier 1 = Highest priority tier (default)
5:1†	RSVD	RW	Reserved. These bits are reserved and must not be changed from their default value of 00000b.
0†	OHCI_TIER_SEL	RW	1394a OHCI tier select. This bit determines in which tier the 1394a OHCI is placed in the arbitration scheme. 0 = Lowest priority tier (default) 1 = Highest priority tier

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Not Recommended for New Designs

4.70 Arbiter Request Mask Register

The arbiter request mask register enables and disables support for requests from specific masters on the secondary bus. The arbiter request mask register also controls if a request input is automatically masked on an arbiter time-out. See Table 4–41 for a complete description of the register contents.

PCI register offset: DDh
Register type: Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 4–41. Arbiter Request Mask Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7†	ARB_TIMEOUT	RW	Arbiter time-out. This bit enables the arbiter time-out feature. The arbiter time-out is defined as the number of PCI clocks after the PCI bus has gone idle for a device to assert $\overline{\text{FRAME}}$ before the arbiter assumes the device will not respond. 0 = Arbiter time disabled (default) 1 = Arbiter time-out set to 16 PCI clocks
6†	AUTO_MASK	RW	Automatic request mask. This bit enables automatic request masking when an arbiter time-out occurs. 0 = Automatic request masking disabled (default) 1 = Automatic request masking enabled
5:1†	RSVD	RW	Reserved. These bits are reserved and must not be changed from their default value of 00000b.
0†	OHCI_MASK	RW	1394a OHCI mask. Setting this bit forces the internal arbiter to ignore requests signaled from the 1394a OHCI. 0 = Use 1394a OHCI request (default) 1 = Ignore 1394a OHCI request

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

4.71 Arbiter Time-Out Status Register

The arbiter time-out status register contains the status of each request (request 5–0) time-out. The time-out status bit for the respective request is set if the device did not assert $\overline{\text{FRAME}}$ after the arbiter time-out value. See Table 4–42 for a complete description of the register contents.

PCI register offset: DEh
Register type: Read/Clear
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 4–42. Arbiter Time-Out Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:1	RSVD	R	Reserved. Returns 000 0000b when read.
0	OHCI_TO	RCU	1394a OHCI request time-out status 0 = No time-out 1 = Time-out has occurred

Not Recommended for New Designs

4.72 TI Proprietary Register

This read/write TI proprietary register is located at offset E0h and controls TI proprietary functions. This register must not be changed from the specified default state. This register is reset by a PCI Express reset ($\overline{PERST}$), a $\overline{GRST}$, or the internally-generated power-on reset.

PCI register offset: E0h
Register type: Read-only, Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

4.73 TI Proprietary Register

This read/write TI proprietary register is located at offset E2h and controls TI proprietary functions. This register must not be changed from the specified default state. This register is reset by a PCI Express reset ($\overline{PERST}$), a $\overline{GRST}$, or the internally-generated power-on reset.

PCI register offset: E2h
Register type: Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

4.74 TI Proprietary Register

This read/clear TI proprietary register is located at offset E4h and controls TI proprietary functions. This register must not be changed from the specified default state.

PCI register offset: E4h
Register type: Read/Clear
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Not Recommended for New Designs

5 PCI Express Extended Configuration Space

The programming model of the PCI Express extended configuration space is compliant to the *PCI Express Base Specification* and the *PCI Express to PCI/PCI-X Bridge Specification* programming models. The PCI Express extended configuration map uses the PCI Express advanced error reporting capability and PCI Express virtual channel (VC) capability headers.

All bits marked with a ☆ are sticky bits and are reset by a global reset ($\overline{GRST}$) or the internally-generated power-on reset. All bits marked with a † are reset by a PCI Express reset ($\overline{PERST}$), a $\overline{GRST}$, or the internally-generated power-on reset. The remaining register bits are reset by a PCI Express hot reset, $\overline{PERST}$, $\overline{GRST}$, or the internally-generated power-on reset.

Table 5–1. PCI Express Extended Configuration Register Map

REGISTER NAME		OFFSET
Next capability offset / capability version	PCI Express advanced error reporting capabilities ID	100h
Uncorrectable error status register†		104h
Uncorrectable error mask register†		108h
Uncorrectable error severity register†		10Ch
Correctable error status register†		110h
Correctable error mask†		114h
Advanced error capabilities and control†		118h
Header log register†		11Ch
Header log register†		120h
Header log register†		124h
Header log register†		128h
Secondary uncorrectable error status†		12Ch
Secondary uncorrectable error mask†		130h
Secondary uncorrectable error severity register†		134h
Secondary error capabilities and control register†		138h
Secondary header log register†		13Ch
Secondary header log register†		140h
Secondary header log register†		144h
Secondary header log register†		148h
Reserved		14Ch
Next capability offset / capability version	PCI express virtual channel extended capabilities ID	150h
Port VC capability register 1		154h
Port VC capability register 2		158h
Port VC status register	Port VC control register	15Ch
VC resource capability register (VC0)		160h
VC resource control register (VC0)		164h
VC resource status register (VC0)	Reserved	168h
VC resource capability register (VC1)		16Ch
VC resource control register (VC1)		170h
VC resource status register (VC1)	Reserved	174h
Reserved		178h – 17Ch
VC arbitration table (phase 7 – phase 0)		180h
VC arbitration table (phase 15 – phase 8)		184h
VC arbitration table (phase 23 – phase 16)		188h

† One or more bits in this register are reset by a PCI Express reset ($\overline{PERST}$), a $\overline{GRST}$, or the internally-generated power-on reset.

Not Recommended for New Designs

Table 5–1. PCI Express Extended Configuration Register Map (Continued)

REGISTER NAME	OFFSET
VC arbitration table (phase 31 – phase 24)	18Ch
Reserved	190h – 1BCh
Port arbitration table for VC1 (phase 7 – phase 0)	1C0h
Port arbitration table for VC1 (phase 15 – phase 8)	1C4h
Port arbitration table for VC1 (phase 23 – phase 16)	1C8h
Port arbitration table for VC1 (phase 31 – phase 24)	1CCh
Port arbitration table for VC1 (phase 39 – phase 32)	1D0h
Port arbitration table for VC1 (phase 47 – phase 40)	1D4h
Port arbitration table for VC1 (phase 55 – phase 48)	1D8h
Port arbitration table for VC1 (phase 63 – phase 56)	1DCh
Port arbitration table for VC1 (phase 71 – phase 64)	1E0h
Port arbitration table for VC1 (phase 79 – phase 72)	1E4h
Port arbitration table for VC1 (phase 87 – phase 80)	1E8h
Port arbitration table for VC1 (phase 95 – phase 88)	1ECh
Port arbitration table for VC1 (phase 103 – phase 96)	1F0h
Port arbitration table for VC1 (phase 111 – phase 104)	1F4h
Port arbitration table for VC1 (phase 119 – phase 112)	1F8h
Port arbitration table for VC1 (phase 127 – phase 120)	1FCh
Reserved	200h – FFCh

† One or more bits in this register are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

5.1 Advanced Error Reporting Capability ID Register

This read-only register identifies the linked list item as the register for PCI Express advanced error reporting capabilities. The register returns 0001h when read.

PCI Express extended register offset: 100h
Register type: Read-only
Default value: 0001h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

5.2 Next Capability Offset/Capability Version Register

This read-only register identifies the next location in the PCI Express extended capabilities link list. If bit 12 (VC_CAP_EN) in the general control register (offset D4h, see Section 4.65) is 0b, then the upper 12 bits in this register are 000h, indicating the end of the linked list. If VC_CAP_EN is 1b, then the upper 12 bits in this register are 150h, indicating the existance of the VC capability structure at offset 150h. The four least significant bits identify the revision of the current capability block as 1h.

PCI Express extended register offset: 102h
Register type: Read-only
Default value: XX01h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	x	0	x	0	x	0	0	0	0	0	0	0	1

Not Recommended for New Designs

5.3 Uncorrectable Error Status Register

The uncorrectable error status register reports the status of individual errors as they occur on the primary PCI Express interface. Software may only clear these bits by writing a 1b to the desired location. See Table 5–2 for a complete description of the register contents.

PCI Express extended register offset: 104h
Register type: Read-only, Read/Clear
Default value: 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5–2. Uncorrectable Error Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:21	RSVD	R	Reserved. Returns 000 0000 0000b when read.
20†	UR_ERROR	RCU	Unsupported request error. This bit is asserted when an unsupported request is received.
19†	ECRC_ERROR	RCU	Extended CRC error. This bit is asserted when an extended CRC error is detected.
18†	MAL_TLP	RCU	Malformed TLP. This bit is asserted when a malformed TLP is detected.
17†	RX_OVERFLOW	RCU	Receiver overflow. This bit is asserted when the flow control logic detects that the transmitting device has illegally exceeded the number of credits that were issued.
16†	UNXP_CPL	RCU	Unexpected completion. This bit is asserted when a completion packet is received that does not correspond to an issued request.
15†	CPL_ABORT	RCU	Completer abort. This bit is asserted when the bridge signals a completer abort.
14†	CPL_TIMEOUT	RCU	Completion time-out. This bit is asserted when no completion has been received for an issued request before the time-out period.
13†	FC_ERROR	RCU	Flow control error. This bit is asserted when a flow control protocol error is detected either during initialization or during normal operation.
12†	PSN_TLP	RCU	Poisoned TLP. This bit is asserted when a poisoned TLP is received.
11:5	RSVD	R	Reserved. Returns 000 0000b when read.
4†	DLL_ERROR	RCU	Data link protocol error. This bit is asserted if a data link layer protocol error is detected.
3:0	RSVD	R	Reserved. Returns 0h when read.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Not Recommended for New Designs

5.4 Uncorrectable Error Mask Register

The uncorrectable error mask register controls the reporting of individual errors as they occur. When a mask bit is set to 1b, the corresponding error status bit is not set, PCI Express error messages are blocked, the header log is not loaded, and the first error pointer is not updated. See Table 5–3 for a complete description of the register contents.

PCI Express extended register offset: 108h
Register type: Read-only, Read/Write
Default value: 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5–3. Uncorrectable Error Mask Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:21	RSVD	R	Reserved. Returns 000 0000 0000b when read.
20†	UR_ERROR_MASK	RW	Unsupported request error mask 0 = Error condition is unmasked (default) 1 = Error condition is masked
19†	ECRC_ERROR_MASK	RW	Extended CRC error mask 0 = Error condition is unmasked (default) 1 = Error condition is masked
18†	MAL_TLP_MASK	RW	Malformed TLP mask 0 = Error condition is unmasked (default) 1 = Error condition is masked
17†	RX_OVERFLOW_MASK	RW	Receiver overflow mask 0 = Error condition is unmasked (default) 1 = Error condition is masked
16†	UNXP_CPL_MASK	RW	Unexpected completion mask 0 = Error condition is unmasked (default) 1 = Error condition is masked
15†	CPL_ABORT_MASK	RW	Completer abort mask 0 = Error condition is unmasked (default) 1 = Error condition is masked
14†	CPL_TIMEOUT_MASK	RW	Completion time-out mask 0 = Error condition is unmasked (default) 1 = Error condition is masked
13†	FC_ERROR_MASK	RW	Flow control error mask 0 = Error condition is unmasked (default) 1 = Error condition is masked
12†	PSN_TLP_MASK	RW	Poisoned TLP mask 0 = Error condition is unmasked (default) 1 = Error condition is masked
11:5	RSVD	R	Reserved. Returns 000 0000b when read.
4†	DLL_ERROR_MASK	RW	Data link protocol error mask 0 = Error condition is unmasked (default) 1 = Error condition is masked
3:0	RSVD	R	Reserved. Returns 0h when read.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Not Recommended for New Designs

5.5 Uncorrectable Error Severity Register

The uncorrectable error severity register controls the reporting of individual errors as ERR_FATAL or ERR_NONFATAL. When a bit is set, the corresponding error condition is identified as fatal. When a bit is cleared, the corresponding error condition is identified as nonfatal. See Table 5–4 for a complete description of the register contents.

PCI Express extended register offset: 10Ch
Register type: Read-only, Read/Write
Default value: 0006 2011h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	1

Table 5–4. Uncorrectable Error Severity Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:21	RSVD	R	Reserved. Returns 000 0000 0000b when read.
20†	UR_ERROR_SEVR	RW	Unsupported request error severity 0 = Error condition is signaled using ERR_NONFATAL (default) 1 = Error condition is signaled using ERR_FATAL
19†	ECRC_ERROR_SEVR	RW	Extended CRC error severity 0 = Error condition is signaled using ERR_NONFATAL (default) 1 = Error condition is signaled using ERR_FATAL
18†	MAL_TLP_SEVR	RW	Malformed TLP severity 0 = Error condition is signaled using ERR_NONFATAL 1 = Error condition is signaled using ERR_FATAL (default)
17†	RX_OVERFLOW_SEVR	RW	Receiver overflow severity 0 = Error condition is signaled using ERR_NONFATAL 1 = Error condition is signaled using ERR_FATAL (default)
16†	UNXP_CPL_SEVR	RW	Unexpected completion severity 0 = Error condition is signaled using ERR_NONFATAL (default) 1 = Error condition is signaled using ERR_FATAL
15†	CPL_ABORT_SEVR	RW	Completer abort severity 0 = Error condition is signaled using ERR_NONFATAL (default) 1 = Error condition is signaled using ERR_FATAL
14†	CPL_TIMEOUT_SEVR	RW	Completion time-out severity 0 = Error condition is signaled using ERR_NONFATAL (default) 1 = Error condition is signaled using ERR_FATAL
13†	FC_ERROR_SEVR	RW	Flow control error severity 0 = Error condition is signaled using ERR_NONFATAL 1 = Error condition is signaled using ERR_FATAL (default)
12†	PSN_TLP_SEVR	RW	Poisoned TLP severity 0 = Error condition is signaled using ERR_NONFATAL (default) 1 = Error condition is signaled using ERR_FATAL
11:5	RSVD	R	Reserved. Returns 000 0000b when read.
4†	DLL_ERROR_SEVR	RW	Data link protocol error severity 0 = Error condition is signaled using ERR_NONFATAL 1 = Error condition is signaled using ERR_FATAL (default)
3:1	RSVD	R	Reserved. Returns 000b when read.
0	RSVD	R	Reserved. Returns 1b when read.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Not Recommended for New Designs

5.6 Correctable Error Status Register

The correctable error status register reports the status of individual errors as they occur. Software may only clear these bits by writing a 1b to the desired location. See Table 5–5 for a complete description of the register contents.

PCI Express extended register offset: 110h
Register type: Read-only, Read/Clear
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5–5. Correctable Error Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:13	RSVD	R	Reserved. Returns 000 0000 0000 0000 0000b when read.
12†	REPLAY_TMOUT	RCU	Replay timer time-out. This bit is asserted when the replay timer expires for a pending request or completion that has not been acknowledged.
11:9	RSVD	R	Reserved. Returns 000b when read.
8†	REPLAY_ROLL	RCU	REPLAY_NUM rollover. This bit is asserted when the replay counter rolls over after a pending request or completion has not been acknowledged.
7†	BAD_DLLP	RCU	Bad DLLP error. This bit is asserted when an 8b/10b error was detected by the PHY during the reception of a DLLP.
6†	BAD_TLP	RCU	Bad TLP error. This bit is asserted when an 8b/10b error was detected by the PHY during the reception of a TLP.
5:1	RSVD	R	Reserved. Returns 00000b when read.
0†	RX_ERROR	RCU	Receiver error. This bit is asserted when an 8b/10b error is detected by the PHY at any time.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Not Recommended for New Designs

5.7 Correctable Error Mask Register

The correctable error mask register controls the reporting of individual errors as they occur. When a mask bit is set to 1b, the corresponding error status bit is not set, PCI Express error messages are blocked, the header log is not loaded, and the first error pointer is not updated. See Table 5–6 for a complete description of the register contents.

PCI Express extended register offset: 114h
Register type: Read-only, Read/Write
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5–6. Correctable Error Mask Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:13	RSVD	R	Reserved. Returns 000 0000 0000 0000 0000b when read.
12†	REPLAY_TMOUT_MASK	RW	Replay timer time-out mask. 0 = Error condition is unmasked (default) 1 = Error condition is masked
11:9	RSVD	R	Reserved. Returns 000b when read.
8†	REPLAY_ROLL_MASK	RW	REPLAY_NUM rollover mask. 0 = Error condition is unmasked (default) 1 = Error condition is masked
7†	BAD_DLLP_MASK	RW	Bad DLLP error mask. 0 = Error condition is unmasked (default) 1 = Error condition is masked
6†	BAD_TLP_MASK	RW	Bad TLP error mask. 0 = Error condition is unmasked (default) 1 = Error condition is masked
5:1	RSVD	R	Reserved. Returns 00000b when read.
0†	RX_ERROR_MASK	RW	Receiver error mask. 0 = Error condition is unmasked (default) 1 = Error condition is masked

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Not Recommended for New Designs

5.8 Advanced Error Capabilities and Control Register

The advanced error capabilities and control register allows the system to monitor and control the advanced error reporting capabilities. See Table 5–7 for a complete description of the register contents.

PCI Express extended register offset: 118h
Register type: Read-only, Read/Write
Default value: 0000 00A0h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0

Table 5–7. Advanced Error Capabilities and Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:9	RSVD	R	Reserved. Returns 000 0000 0000 0000 0000 0000b when read.
8†	ECRC_CHK_EN	RW	Extended CRC check enable 0 = Extended CRC checking is disabled 1 = Extended CRC checking is enabled
7	ECRC_CHK_CAPABLE	R	Extended CRC check capable. This read-only bit returns a value of 1b indicating that the bridge is capable of checking extended CRC information.
6†	ECRC_GEN_EN	RW	Extended CRC generation enable 0 = Extended CRC generation is disabled 1 = Extended CRC generation is enabled
5	ECRC_GEN_CAPABLE	R	Extended CRC generation capable. This read-only bit returns a value of 1b indicating that the bridge is capable of generating extended CRC information.
4:0†	FIRST_ERR	RU	First error pointer. This 5-bit value reflects the bit position within the uncorrectable error status register (offset 104h, see Section 5.3) corresponding to the class of the first error condition that was detected.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

5.9 Header Log Register

The header log register stores the TLP header for the packet that lead to the most recently detected error condition. Offset 11Ch contains the first DWORD. Offset 128h contains the last DWORD (in the case of a 4DW TLP header). Each DWORD is stored with the least significant byte representing the earliest transmitted. These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

PCI Express extended register offset: 11Ch, 120h, 124h, and 128h
Register type: Read-only
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Not Recommended for New Designs

5.10 Secondary Uncorrectable Error Status Register

The secondary uncorrectable error status register reports the status of individual PCI bus errors as they occur. Software may only clear these bits by writing a 1b to the desired location. See Table 5–8 for a complete description of the register contents.

PCI Express extended register offset: 12Ch
Register type: Read-only, Read/Clear
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5–8. Secondary Uncorrectable Error Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:13	RSVD	R	Reserved. Returns 000 0000 0000 0000 0000b when read.
12†	SERR_DETECT	RCU	$\overline{\text{SERR}}$ assertion detected. This bit is asserted when the bridge detects the assertion of $\overline{\text{SERR}}$ on the secondary bus.
11†	PERR_DETECT	RCU	$\overline{\text{PERR}}$ assertion detected. This bit is asserted when the bridge detects the assertion of $\overline{\text{PERR}}$ on the secondary bus.
10†	DISCARD_TIMER	RCU	Delayed transaction discard timer expired. This bit is asserted when the discard timer expires for a pending delayed transaction that was initiated on the secondary bus.
9†	UNCOR_ADDR	RCU	Uncorrectable address error. This bit is asserted when the bridge detects a parity error during the address phase of an upstream transaction.
8	RSVD	R	Reserved. Returns 0b when read.
7†	UNCOR_DATA	RCU	Uncorrectable data error. This bit is asserted when the bridge detects a parity error during a data phase of an upstream write transaction, or when the bridge detects the assertion of $\overline{\text{PERR}}$ when forwarding read completion data to a PCI device.
6:4	RSVD	R	Reserved. Returns 000b when read.
3†	MASTER_ABORT	RCU	Received master abort. This bit is asserted when the bridge receives a master abort on the PCI interface.
2†	TARGET_ABORT	RCU	Received target abort. This bit is asserted when the bridge receives a target abort on the PCI interface.
1:0	RSVD	R	Reserved. Returns 00b when read.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Not Recommended for New Designs

5.11 Secondary Uncorrectable Error Mask Register

The secondary uncorrectable error mask register controls the reporting of individual errors as they occur. When a mask bit is set to 1b, the corresponding error status bit is not set, PCI Express error messages are blocked, the header log is not loaded, and the first error pointer is not updated. See Table 5–9 for a complete description of the register contents.

PCI Express extended register offset: 130h
Register type: Read-only, Read/Write
Default value: 0000 17A8h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	1	0	1	1	1	1	0	1	0	1	0	0	0

Table 5–9. Secondary Uncorrectable Error Mask Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:14	RSVD	R	Reserved. Returns 00 0000 0000 0000 0000b when read.
13†	BRIDGE_ERROR_MASK	RW	Internal bridge error. This mask bit is associated with a PCI-X error and has no effect on the bridge.
12†	SERR_DETECT_MASK	RW	$\overline{\text{SERR}}$ assertion detected 0 = Error condition is unmasked 1 = Error condition is masked (default)
11†	PERR_DETECT_MASK	RW	$\overline{\text{PERR}}$ assertion detected 0 = Error condition is unmasked (default) 1 = Error condition is masked
10†	DISCARD_TIMER_MASK	RW	Delayed transaction discard timer expired 0 = Error condition is unmasked 1 = Error condition is masked (default)
9†	UNCOR_ADDR_MASK	RW	Uncorrectable address error 0 = Error condition is unmasked 1 = Error condition is masked (default)
8†	ATTR_ERROR_MASK	RW	Uncorrectable attribute error. This mask bit is associated with a PCI-X error and has no effect on the bridge.
7†	UNCOR_DATA_MASK	RW	Uncorrectable data error 0 = Error condition is unmasked 1 = Error condition is masked (default)
6†	SC_MSG_DATA_MASK	RW	Uncorrectable split completion message data error. This mask bit is associated with a PCI-X error and has no effect on the bridge.
5†	SC_ERROR_MASK	RW	Unexpected split completion error. This mask bit is associated with a PCI-X error and has no effect on the bridge.
4	RSVD	R	Reserved. Returns 0b when read.
3†	MASTER_ABORT_MASK	RW	Received master abort 0 = Error condition is unmasked 1 = Error condition is masked (default)
2†	TARGET_ABORT_MASK	RW	Received target abort 0 = Error condition is unmasked (default) 1 = Error condition is masked
1†	SC_MSTR_ABORT_MASK	RW	Master abort on split completion. This mask bit is associated with a PCI-X error and has no effect on the bridge.
0	RSVD	R	Reserved. Returns 0b when read.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Not Recommended for New Designs

5.12 Secondary Uncorrectable Error Severity Register

The uncorrectable error severity register controls the reporting of individual errors as ERR_FATAL or ERR_NONFATAL. When a bit is set, the corresponding error condition is identified as fatal. When a bit is cleared, the corresponding error condition is identified as nonfatal. See Table 5–10 for a complete description of the register contents.

PCI Express extended register offset: 134h
Register type: Read-only, Read/Write
Default value: 0000 1340h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	1	0	0	1	1	0	1	0	0	0	0	0	0

Table 5–10. Secondary Uncorrectable Error Severity Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:14	RSVD	R	Reserved. Returns 00 0000 0000 0000 0000b when read.
13†	BRIDGE_ERROR_SEVR	RW	Internal bridge error. This severity bit is associated with a PCI-X error and has no effect on the bridge.
12†	SERR_DETECT_SEVR	RW	$\overline{\text{SERR}}$ assertion detected 0 = Error condition is signaled using ERR_NONFATAL 1 = Error condition is signaled using ERR_FATAL (default)
11†	PERR_DETECT_SEVR	RW	$\overline{\text{PERR}}$ assertion detected 0 = Error condition is signaled using ERR_NONFATAL (default) 1 = Error condition is signaled using ERR_FATAL
10†	DISCARD_TIMER_SEVR	RW	Delayed transaction discard timer expired 0 = Error condition is signaled using ERR_NONFATAL (default) 1 = Error condition is signaled using ERR_FATAL
9†	UNCOR_ADDR_SEVR	RW	Uncorrectable address error 0 = Error condition is signaled using ERR_NONFATAL 1 = Error condition is signaled using ERR_FATAL (default)
8†	ATTR_ERROR_SEVR	RW	Uncorrectable attribute error. This severity bit is associated with a PCI-X error and has no effect on the bridge.
7†	UNCOR_DATA_SEVR	RW	Uncorrectable data error 0 = Error condition is signaled using ERR_NONFATAL (default) 1 = Error condition is signaled using ERR_FATAL
6†	SC_MSG_DATA_SEVR	RW	Uncorrectable split completion message data error. This severity bit is associated with a PCI-X error and has no effect on the bridge.
5†	SC_ERROR_SEVR	RW	Unexpected split completion error. This severity bit is associated with a PCI-X error and has no effect on the bridge.
4	RSVD	R	Reserved. Returns 0b when read.
3†	MASTER_ABORT_SEVR	RW	Received master abort 0 = Error condition is signaled using ERR_NONFATAL (default) 1 = Error condition is signaled using ERR_FATAL
2†	TARGET_ABORT_SEVR	RW	Received target abort 0 = Error condition is signaled using ERR_NONFATAL (default) 1 = Error condition is signaled using ERR_FATAL
1†	SC_MSTR_ABORT_SEVR	RW	Master abort on split completion. This severity bit is associated with a PCI-X error and has no effect on the bridge.
0	RSVD	R	Reserved. Returns 0b when read.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Not Recommended for New Designs

5.13 Secondary Error Capabilities and Control Register

The secondary error capabilities and control register allows the system to monitor and control the secondary advanced error reporting capabilities. See Table 5–11 for a complete description of the register contents.

PCI Express extended register offset: 138h
Register type: Read-only
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5–11. Secondary Error Capabilities and Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:5	RSVD	R	Reserved. Return 000 0000 0000 0000 0000 0000 0000b when read.
4:0†	SEC_FIRST_ERR	RU	First error pointer. This 5-bit value reflects the bit position within the secondary uncorrectable error status register (offset12Ch, see Section 5.10) corresponding to the class of the first error condition that was detected.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Not Recommended for New Designs

5.14 Secondary Header Log Register

The secondary header log register stores the transaction address and command for the PCI bus cycle that led to the most recently detected error condition. Offset 13Ch accesses register bits 31:0. Offset 140h accesses register bits 63:32. Offset 144h accesses register bits 95:64. Offset 148h accesses register bits 127:96. See Table 5–12 for a complete description of the register contents.

PCI Express extended register offset: 13Ch, 140h, 144h, and 148h
Register type: Read-only
Default value: 0000 0000h

BIT NUMBER	127	126	125	124	123	122	121	120	119	118	117	116	115	114	113	112
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	111	110	109	108	107	106	105	104	103	102	101	100	99	98	97	96
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5–12. Secondary Header Log Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
127:64†	ADDRESS	RU	Transaction address. The 64-bit value transferred on AD[31:0] during the first and second address phases. The first address phase is logged to 95:64 and the second address phase is logged to 127:96. In the case of a 32-bit address, bits 127:96 are set to 0.
63:44	RSVD	R	Reserved. Returns 0 0000h when read.
43:40†	UPPER_CMD	RU	Transaction command upper. Contains the status of the C/$\overline{BE}$ terminals during the second address phase of the PCI transaction that generated the error if using a dual-address cycle.
39:36†	LOWER_CMD	RU	Transaction command lower. Contains the status of the C/$\overline{BE}$ terminals during the first address phase of the PCI transaction that generated the error.
35:0	TRANS_ATTRIBUTE	R	Transaction attribute. Because the bridge does not support the PCI-X attribute transaction phase, these bits have no function, and return 0 0000 0000h when read.

† These bits are reset by a PCI Express reset ($\overline{PERST}$), a $\overline{GRST}$, or the internally-generated power-on reset.

5.15 Virtual Channel Capability ID Register

This read-only register identifies the linked list item as the register for PCI Express VC capabilities. The register returns 0002h when read.

PCI Express extended register offset: 150h
Register type: Read-only
Default value: 0002h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Not Recommended for New Designs

5.16 Next Capability Offset/Capability Version Register

This read-only register returns the value 000h to indicate that this extended capability block represents the end of the linked list of extended capability structures. The four least significant bits identify the revision of the current capability block as 1h.

PCI Express extended register offset: 152h
Register type: Read-only
Default value: 0001h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

5.17 Port VC Capability Register 1

The first port VC capability register provides information to software regarding the VC capabilities support by the bridge. See Table 5–13 for a complete description of the register contents.

PCI Express extended register offset: 154h
Register type: Read-only
Default value: 0000 08X1h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	1	0	0	0	0	0	0	x	0	0	0	1

Table 5–13. Port VC Capability Register 1 Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:12	RSVD	R	Reserved. Returns 00000h when read.
11:10	PORT_TABLE_SIZE	R	Port arbitration table entry size. This read-only field returns a value of 10b to indicate that the field size within the port arbitration table is four bits. This is necessary to allow as many as six secondary PCI bus masters.
9:8	REF_CLK	R	Reference clock. This read-only field returns a value of 00b to indicate than an internal 100-ns timer is used for time-based, WRR port arbitration.
7	RSVD	R	Reserved. Returns 0b when read.
6:4	LOW_PRIORITY_COUNT	RU	Low priority extended VC count. When bit 25 (STRICT_PRIORITY_EN) in the general control register (offset D4h, see Section 4.65) is 0b, the default LOW_PRIORITY_COUNT is 001b. When STRICT_PRIORITY_EN is 1b, the default LOW_PRIORITY_COUNT is 000b. When STRICT_PRIORITY_EN is set, strict priority VC arbitration is used and the extended VC always receives priority over VC0 at the PCI Express port.
3	RSVD	R	Reserved. Returns 0b when read.
2:0	EXT_VC_COUNT	R	Extended VC count. This read-only field returns a value of 001b to indicate support for one extended VC.

Not Recommended for New Designs

5.18 Port VC Capability Register 2

The second port VC capability register provides information to software regarding the VC arbitration schemes supported by the bridge. See Table 5–14 for a complete description of the register contents.

PCI Express extended register offset: 158h
Register type: Read-only
Default value: 0X00 000Xh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	x	x	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x	x

Table 5–14. Port VC Capability Register 2 Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:24	VC_ARB_ TBL_OFFSET	RU	VC arbitration table offset. If bits 6:4 (LOW_PRIORITY_COUNT) in the port VC capability register 1 (offset 154h, see Section 5.17) are 000b, then this field returns 00h when read. Otherwise, this read-only field returns the value 03h to indicate that the VC arbitration table begins 48 bytes from the top of the VC capability structure. When this field equals 00h, the VC arbitration table is a scratch pad and has no effect in the bridge.
23:8	RSVD	R	Reserved. Returns 0000h when read.
7:0	VC_ARB _CAP	RU	VC arbitration capability. This 8-bit encoded field indicates support for the various schemes that are supported for VC arbitration. The field is encoded as follows: Bit 0 = Hardware fixed arbitration (round-robin) Bit 1 = WRR with 32 phases Bit 2 = WRR with 64 phases Bit 3 = WRR with 128 phases Bit 4 = Reserved Bit 5 = Reserved Bit 6 = Reserved Bit 7 = Reserved If bits 6:4 (LOW_PRIORITY_COUNT) in the port VC capability register 1 (offset 154h, see Section 5.17) are 000b, then this field returns 00h when read. Otherwise, this field returns 03h to indicate that hardware-fixed round-robin and WRR with 32 phases are both supported.

Not Recommended for New Designs

5.19 Port VC Control Register

The port VC control register allows software to configure the VC arbitration options within the bridge. See Table 5–15 for a complete description of the register contents.

PCI Express extended register offset: 15Ch
Register type: Read-only, Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5–15. Port VC Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	RSVD	R	Reserved. Returns 000h when read.
3:1	VC_ARB _SELECT	RW	VC arbitration select. This read/write field allows software to define the mechanism used for VC arbitration by the bridge. The value written to this field indicates the bit position within bits 7:0 (VC_ARB_CAP) in the port VC capability register 2 (offset 158h, see Section 5.18) that corresponds to the selected arbitration scheme. Values that may be written to this field include: 000 = Hardware-fixed round-robin (default) 001 = WRR with 32 phases All other values are reserved for arbitrations schemes that are not supported by the bridge.
0	LOAD_VC _TABLE	RW	Load VC arbitration table. When software writes a 1b to this bit, the bridge applies the values written in the VC arbitration table within the extended configuration space to the actual VC arbitration tables used by the device for arbitration. This bit always returns 0b when read.

5.20 Port VC Status Register

The port VC status register allows software to monitor the status of the VC arbitration table. See Table 5–16 for a complete description of the register contents.

PCI Express extended register offset: 15Eh
Register type: Read-only
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5–16. Port VC Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:1	RSVD	R	Reserved. Returns 000 0000 0000 0000b when read.
0	VC_TABLE_STATUS	RU	VC arbitration table status. This bit is automatically set by hardware when any modification is made to the VC arbitration table entries within the extended configuration space. This bit is cleared by hardware after software has requested a VC arbitration table refresh and the refresh has been completed.

Not Recommended for New Designs

5.21 VC Resource Capability Register (VC0)

The VC resource capability register for VC0 provides information to software regarding the port and arbitration schemes supported by the bridge. See Table 5–17 for a complete description of the register contents.

PCI Express extended register offset: 160h
Register type: Read-only
Default value: 0000 0001h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Table 5–17. VC Resource Capability Register (VC0) Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:24	PORT_ARB_TBL_OFFSET	R	Port arbitration table offset. This read-only field returns the value 00h to indicate that no port arbitration table is required for this VC.
23	RSVD	R	Reserved. Returns 0b when read.
22:16	MAX_TIME_SLOTS	R	Maximum time slots. The read-only field returns the value 00h because there is no support for time-based, WRR arbitration on this VC.
15	REJECT_SNOOP	R	Reject snoop transactions. This bit only has meaningful context for root ports and therefore returns 0b when read.
14	ADV_SWITCHING	R	Advanced packet switching. This read-only bit returns 0b to indicate that the use of this VC is not limited to AS traffic.
13:8	RSVD	R	Reserved. Returns 00 0000b when read.
7:0	PORT_ARB_CAP	R	Port arbitration capability. This 8-bit encoded field indicates support for the various schemes that are supported for port (secondary PCI device) arbitration. The field is encoded as follows: Bit 0 = Hardware fixed arbitration (round-robin) Bit 1 = WRR with 32 phases Bit 2 = WRR with 64 phases Bit 3 = WRR with 128 phases Bit 4 = Time-based WRR with 128 phases Bit 5 = WRR with 256 phases Bit 6 = Reserved Bit 7 = Reserved The returned value of 01h indicates that only hardware-fixed, round-robin arbitration is supported for this VC.

Not Recommended for New Designs

5.22 VC Resource Control Register (VC0)

The VC resource control register for VC0 allows software to control VC0 and the associated port and arbitration schemes supported by the bridge. See Table 5–18 for a complete description of the register contents.

PCI Express extended register offset: 164h
Register type: Read-only, Read/Write
Default value: 8000 00FFh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Table 5–18. VC Resource Control Register (VC0) Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31	VC_EN	R	VC enable. This field is internally hardwired to 1b to indicate that this VC resource is always enabled.
30:27	RSVD	R	Reserved. Returns 0h when read.
26:24	VC_ID	R	Virtual channel ID. This field is internally hardwired to 000b to indicate that this VC resource is always used for VC0.
23:20	RSVD	R	Reserved. Returns 0h when read.
19:17	PORT_ARB_SELECT	R	Port arbitration select. This read-only field returns 000b when read, because only hardware-fixed, round-robin arbitration is supported for this VC.
16	LOAD_PORT_TABLE	R	Load port arbitration table. This read-only bit returns 0b when read, because no port arbitration table is supported for this VC.
15:8	RSVD	R	Reserved. Returns 00h when read.
7:0	TC_VC_MAP	RW	TC/VC map. This field indicates all of the traffic classes that are mapped to this VC. A 1b in any bit position indicates that the corresponding traffic class is enabled for this VC. A 0b indicates that the corresponding traffic class is mapped to a different VC. The following table is used: Bit 0 = Traffic class 0 (This bit is read-only and returns a value of 1b) Bit 1 = Traffic class 1 Bit 2 = Traffic class 2 Bit 3 = Traffic class 3 Bit 4 = Traffic class 4 Bit 5 = Traffic class 5 Bit 6 = Traffic class 6 Bit 7 = Traffic class 7 The default value of FFh indicates that all eight traffic classes are initially mapped to VC0.

Not Recommended for New Designs

5.23 VC Resource Status Register (VC0)

The VC resource status register allows software to monitor the status of the port arbitration table for this VC. See Table 5–19 for a complete description of the register contents.

PCI Express extended register offset: 16Ah
Register type: Read-only
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5–19. VC Resource Status Register (VC0) Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:2	RSVD	R	Reserved. Returns 00 0000 0000 0000b when read.
1	VC_PENDING	RU	VC negotiation pending. This bit is asserted when VC negotiation is in progress following a request by software to enable or disable the VC or at startup for VC0.
0	PORT_TABLE_STATUS	RU	Port arbitration table status. This bit is automatically set by hardware when any modification is made to the port arbitration table entries for this VC within the extended configuration space. This bit is cleared by hardware after software has requested a port arbitration table refresh and the refresh has been completed.

Not Recommended for New Designs

5.24 VC Resource Capability Register (VC1)

The VC resource capability register for VC1 provides information to software regarding the port and arbitration schemes supported by the bridge. See Table 5–20 for a complete description of the register contents.

PCI Express extended register offset: 16Ch
Register type: Read-only
Default value: 077F 0011h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1

Table 5–20. VC Resource Capability Register (VC1) Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31:24	PORT_ARB_ TBL_OFFSET	R	Port arbitration table offset. This read-only field returns the value 07h to indicate that the port arbitration table for this VC begins 112 bytes from the top of the VC capability structure.
23	RSVD	R	Reserved. Returns 0b when read.
22:16	MAX_TIME_ SLOTS	R	Maximum time slots. The read-only field returns the value 7Fh to indicate that all 128 slots are supported for time-based WRR.
15	REJECT_ SNOOP	R	Reject snoop transactions. This bit only has meaningful context for root ports and therefore returns 0b when read.
14	ADV_ SWITCHING	R	Advanced packet switching. This read-only bit returns the value 0b to indicate that the use of this VC is not limited to AS traffic.
13:8	RSVD	R	Reserved. Returns 00 0000b when read.
7:0	PORT_ ARB_CAP	R	Port arbitration capability. This 8-bit encoded field indicates support for the various schemes that are supported for port (secondary PCI device) arbitration. The field is encoded as follows: Bit 0 = Hardware fixed arbitration (round-robin) Bit 1 = WRR with 32 phases Bit 2 = WRR with 64 phases Bit 3 = WRR with 128 phases Bit 4 = Time-based WRR with 128 phases Bit 5 = WRR with 256 phases Bit 6 = Reserved Bit 7 = Reserved The returned value of 11h indicates that hardware-fixed round-robin and time-based WRR with 128 phases are both supported.

Not Recommended for New Designs

5.25 VC Resource Control Register (VC1)

The VC resource control register for VC1 allows software to control the second VC and associated port and arbitration schemes supported by the bridge. See Table 5–21 for a complete description of the register contents.

PCI Express extended register offset: 170h
Register type: Read-only, Read/Write
Default value: 0100 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5–21. VC Resource Control Register (VC1) Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
31	VC_EN	RW	VC enable. This bit is used by software to enable this VC resource. Writing a 1b to this bit causes the bridge to begin VC negotiation and set bit 1 (VC_PENDING) in the VC resource status register for this VC (offset 176h, see Section 5.26). The default value for this bit is 0b.
30:27	RSVD	R	Reserved. Returns 0h when read.
26:24	VC_ID	RW	Virtual channel ID. This field allows software to assign a VC ID to this VC resource. Valid values range from 001b to 111b, because the value 000b is hardware-fixed to VC0 within the device. The default value for this field is 001b.
23:20	RSVD	R	Reserved. Returns 0h when read.
19:17	PORT_ARB _SELECT	RW	Port arbitration select. This read/write field allows software to define the mechanism used for port arbitration by the bridge on this VC. The value written to this field indicates the bit position within bits 7:0 (PORT_ARB_CAP) in the VC resource capability register for this VC (offset 16Ch, see Section 5.24) that corresponds to the selected arbitration scheme. Values that may be written to this field include: 000 = Hardware-fixed round-robin (default) 100 = Time-based WRR with 128 phases All other values are reserved for arbitrations schemes that are not supported by the bridge.
16	LOAD_PORT _TABLE	RW	Load port arbitration table. When software writes a 1b to this bit, the bridge applies the values written in the port arbitration table for this VC within the extended configuration space to the actual port arbitration tables used by the device for arbitration on this VC. This bit always returns 0b when read.
15:8	RSVD	R	Reserved. Returns 00h when read.
7:0	TC_VC_MAP	RW	TC/VC map. This field indicates all of the traffic classes that are mapped to this VC. A 1b in any bit position indicates that the corresponding traffic class is enabled for this VC. A 0b indicates that the corresponding traffic class is mapped to a different VC. The following table is used: Bit 0 = Traffic class 0 (This bit is read only and returns a value of 0b) Bit 1 = Traffic class 1 Bit 2 = Traffic class 2 Bit 3 = Traffic class 3 Bit 4 = Traffic class 4 Bit 5 = Traffic class 5 Bit 6 = Traffic class 6 Bit 7 = Traffic class 7 The default value of 00h indicates that none of the eight traffic classes are initially mapped to this VC.

Not Recommended for New Designs

5.26 VC Resource Status Register (VC1)

The VC resource status register allows software to monitor the status of the port arbitration table for this VC. See Table 5–22 for a complete description of the register contents.

PCI Express extended register offset: 176h
Register type: Read-only
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5–22. VC Resource Status Register (VC1) Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:2	RSVD	R	Reserved. Returns 00 0000 0000 0000b when read.
1	VC_PENDING	RU	VC negotiation pending. This bit is asserted when VC negotiation is in progress following a request by software to enable the second VC.
0	PORT_TABLE _STATUS	RU	Port arbitration table status. This bit is automatically set by hardware when any modification is made to the port arbitration table entries for this VC within the extended configuration space. This bit is cleared by hardware after software has requested a port arbitration table refresh and the refresh has been completed.

5.27 VC Arbitration Table

The VC arbitration table is provided to allow software to define round-robin weighting for traffic targeting the PCI Express port. The table is divided into 32 phases. See Table 5–24 for a complete description of the register contents.

PCI Express extended register offset: 180h – 18Ch
Register type: Read-only, Read/Write
Default value: 0000 0000h

Table 5–23. VC Arbitration Table

REGISTER FORMAT								OFFSET
Phase 7	Phase 6	Phase 5	Phase 4	Phase 3	Phase 2	Phase 1	Phase 0	180h
Phase 15	Phase 14	Phase 13	Phase 12	Phase 11	Phase 10	Phase 9	Phase 8	184h
Phase 23	Phase 22	Phase 21	Phase 20	Phase 19	Phase 18	Phase 17	Phase 16	188h
Phase 31	Phase 30	Phase 29	Phase 28	Phase 27	Phase 26	Phase 25	Phase 24	18Ch

Each phase consists of a four-bit field as indicated below.

BIT NUMBER	3	2	1	0
RESET STATE	0	0	0	0

Table 5–24. VC Arbitration Table Entry Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
3	RSVD	R	Reserved. Returns 0b when read.
2:0	VC_ARB_ID	RW	Virtual channel ID. This 3-bit field is used by software to identify the VC ID that must be allocated to this slot of arbitration bandwidth depending upon the VC arbitration scheme enabled. The default value for this field is 000b.

Not Recommended for New Designs

5.28 Port Arbitration Table (VC1)

The port arbitration table is provided to allow software to define round-robin weighting for traffic entering the PCI interface. The table is divided into 128 phases. See Table 5–26 for a complete description of the register contents.

PCI Express extended register offset: 1C0h – 1FCh
Register type: Read/Write
Default value: 0000 0000h

Table 5–25. Port Arbitration Table

REGISTER FORMAT								OFFSET
Phase 7	Phase 6	Phase 5	Phase 4	Phase 3	Phase 2	Phase 1	Phase 0	1C0h
Phase 15	Phase 14	Phase 13	Phase 12	Phase 11	Phase 10	Phase 9	Phase 8	1C4h
Phase 23	Phase 22	Phase 21	Phase 20	Phase 19	Phase 18	Phase 17	Phase 16	1C8h
Phase 31	Phase 30	Phase 29	Phase 28	Phase 27	Phase 26	Phase 25	Phase 24	1CCh
Phase 39	Phase 38	Phase 37	Phase 36	Phase 35	Phase 34	Phase 33	Phase 32	1D0h
Phase 47	Phase 46	Phase 45	Phase 44	Phase 43	Phase 42	Phase 41	Phase 40	1D4h
Phase 55	Phase 54	Phase 53	Phase 52	Phase 51	Phase 50	Phase 49	Phase 48	1D8h
Phase 63	Phase 62	Phase 61	Phase 60	Phase 59	Phase 58	Phase 57	Phase 56	1DCh
Phase 71	Phase 70	Phase 69	Phase 68	Phase 67	Phase 66	Phase 65	Phase 64	1E0h
Phase 79	Phase 78	Phase 77	Phase 76	Phase 75	Phase 74	Phase 73	Phase 72	1E4h
Phase 87	Phase 86	Phase 85	Phase 84	Phase 83	Phase 82	Phase 81	Phase 80	1E8h
Phase 95	Phase 94	Phase 93	Phase 92	Phase 91	Phase 90	Phase 89	Phase 88	1ECh
Phase 103	Phase 102	Phase 101	Phase 100	Phase 99	Phase 98	Phase 97	Phase 96	1F0h
Phase 111	Phase 110	Phase 109	Phase 108	Phase 107	Phase 106	Phase 105	Phase 104	1F4h
Phase 119	Phase 118	Phase 117	Phase 116	Phase 115	Phase 114	Phase 113	Phase 112	1F8h
Phase 127	Phase 126	Phase 125	Phase 124	Phase 123	Phase 122	Phase 121	Phase 120	1FCh

Each phase consists of a four-bit field as indicated below.

BIT NUMBER	3	2	1	0
RESET STATE	0	0	0	0

Table 5–26. Port Arbitration Table Entry Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
3:0	PORT_SELECT	RW	Port arbitration select. This 4-bit field is used by software to identify the port ID (secondary PCI device) that must be allocated to this slot of arbitration bandwidth depending upon the port arbitration scheme enabled. The default value for this field is 0h.

Not Recommended for New Designs

6 Memory-Mapped TI Proprietary Register Space

The programming model of the memory-mapped TI proprietary register space is unique to this device. These custom registers are specifically designed to provide enhanced features associated with upstream isochronous applications.

All bits marked with a ☆ are sticky bits and are reset by a global reset ($\overline{GRST}$) or the internally-generated power-on reset. All bits marked with a † are reset by a PCI Express reset ($\overline{PERST}$), a $\overline{GRST}$, or the internally-generated power-on reset. The remaining register bits are reset by a PCI Express hot reset, $\overline{PERST}$, $\overline{GRST}$, or the internally-generated power-on reset.

Table 6–1. Device Control Memory Window Register Map

REGISTER NAME				OFFSET
Upstream isochrony capabilities		Revision ID	Device control map ID	00h
Reserved		Upstream isochrony control		04h
Reserved		Upstream isochronous window 0 control		08h
Upstream isochronous window 0 base address				0Ch
Upstream isochronous window 0 limit				10h
Reserved		Upstream isochronous window 1 control		14h
Upstream isochronous window 1 base address				18h
Upstream isochronous window 1 limit				1Ch
Reserved		Upstream isochronous window 2 control		20h
Upstream isochronous window 2 base address				24h
Upstream isochronous window 2 limit				28h
Reserved		Upstream isochronous window 3 control		2Ch
Upstream isochronous window 3 base address				30h
Upstream isochronous window 3 limit				34h
Reserved				38h–3Ch
GPIO data†		GPIO control†		40h
Serial-bus control and status†	Serial-bus slave address†	Serial-bus word address†	Serial-bus data†	44h
TI proprietary†		Reserved	TI proprietary†	48h
Reserved		TI proprietary		4Ch

† One or more bits in this register are reset by a PCI Express reset ($\overline{PERST}$), a $\overline{GRST}$, or the internally-generated power-on reset.

6.1 Device Control Map ID Register

The device control map ID register identifies the TI proprietary layout for this device control map. The value 01h identifies this as a PCI Express-to-PCI bridge supporting upstream isochronous capabilities.

Device control memory window register offset: 00h
Register type: Read-only
Default value: 01h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	1

6.2 Revision ID Register

The revision ID register identifies the revision of the TI proprietary layout for this device control map. The value 00h identifies the revision as the initial layout.

Device control memory window register offset: 01h
Register type: Read-only
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Not Recommended for New Designs

6.3 Upstream Isochrony Capabilities Register

The upstream isochronous capabilities register provides software information regarding the capabilities supported by this bridge. See Table 6–2 for a complete description of the register contents.

Device control memory window register offset: 02h
Register type: Read-only
Default value: 0004h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Table 6–2. Upstream Isochronous Capabilities Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	RSVD	R	Reserved. Returns 000h when read.
3:0	ISOC_WINDOW_COUNT	R	Isochronous window count. This 4-bit field indicates the number of isochronous address windows supported. The value 0100b indicates that 4 separate windows are supported by the bridge.

6.4 Upstream Isochrony Control Register

The upstream isochrony control register allows software to control bridge isochronous behavior. See Table 6–3 for a complete description of the register contents.

Device control memory window register offset: 04h
Register type: Read-only, Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6–3. Upstream Isochrony Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:3	RSVD	R	Reserved. Returns 0 0000 0000 0000b when read.
2	PORTARB_LEVEL_2_EN	RW	Port arbitration level 2 enable. This bit is only valid if PORTARB_LEVEL_1_EN is set to 1b, because this enhances the behavior enabled through the assertion of that bit. If PORTARB_LEVEL_1_EN is clear, then this bit is read-only and returns 0b when read. 0 = Arbiter behavior follows PORTARB_LEVEL_1_EN rules (default) 1 = Aggressive mode. The arbiter deliberately stops secondary bus masters in the middle of their transaction to assure that isochrony is preserved.
1	PORTARB_LEVEL_1_EN	RW	Port arbitration level 1 enable. 0 = Arbiter behavior is controlled only by the arbiter control registers within the classic PCI configuration space (default) 1 = Values programmed within the port arbitration table for extended VCs impact the arbiter's decision to assert $\overline{GNT}$ to any particular bus master. Programmed values in the arbiter control registers within the classic PCI configuration space have no effect when this bit is asserted.
0	ISOC_ENABLE	RW	Isochronous enable. Global enable bit for the upstream isochronous capability of the bridge. 0 = Mapping of upstream traffic to TCs other than TC0 prohibited (default) 1 = Mapping of upstream traffic to TCs other than TC0 permitted

Not Recommended for New Designs

6.5 Upstream Isochronous Window 0 Control Register

The upstream isochronous window 0 control register allows software to identify the traffic class (TC) associated with upstream transactions targeting memory addresses in the range defined by the window. See Table 6–4 for a complete description of the register contents.

Device control memory window register offset: 08h
Register type: Read-only, Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6–4. Upstream Isochronous Window 0 Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	RSVD	R	Reserved. Returns 000h when read.
3:1	TC_ID	RW	Traffic class ID. ID of the traffic class that upstream transactions targeting the range defined by the associated window must be mapped to. The default value for this field is 000b.
0	ISOC_WINDOW_EN	RW	Isochronous window enable 0 = Address window does not impact upstream traffic (default) 1 = Upstream transactions targeting addresses within the range of this window are applied to the appropriate TC

6.6 Upstream Isochronous Window 0 Base Address Register

The upstream isochronous window 0 base address register allows software to configure the base address for this upstream isochronous window. The entire 32-bit field is read/write and acts as scratchpad space if the window is disabled.

Device control memory window register offset: 0Ch
Register type: Read/Write
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.7 Upstream Isochronous Window 0 Limit Register

The upstream isochronous window 0 limit register allows software to configure the upper address bound for this upstream isochronous window. The entire 32-bit field is read/write and acts as scratchpad space if the window is disabled.

Device control memory window register offset: 10h
Register type: Read/Write
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Not Recommended for New Designs

6.8 Upstream Isochronous Window 1 Control Register

The upstream isochronous window 1 control register allows software to identify the TC associated with upstream transactions targeting memory addresses in the range defined by the window. See Table 6–5 for a complete description of the register contents.

Device control memory window register offset: 14h
Register type: Read-only, Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6–5. Upstream Isochronous Window 1 Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	RSVD	R	Reserved. Returns 000h when read.
3:1	TC_ID	RW	Traffic class ID. ID of the traffic class that upstream transactions targeting the range defined by the associated window must be mapped to. The default value for this field is 000b.
0	ISOC_WINDOW_EN	RW	Isochronous window enable. 0 = Address window does not impact upstream traffic (default) 1 = Upstream transactions targeting addresses within the range of this window are applied to the appropriate TC

6.9 Upstream Isochronous Window 1 Base Address Register

The upstream isochronous window 1 base address register allows software to configure the base address for this upstream isochronous window. The entire 32-bit field is read/write and acts as scratchpad space if the window is disabled.

Device control memory window register offset: 18h
Register type: Read/Write
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.10 Upstream Isochronous Window 1 Limit Register

The upstream isochronous window 1 limit register allows software to configure the upper address bound for this upstream isochronous window. The entire 32-bit field is read/write and acts as scratchpad space if the window is disabled.

Device control memory window register offset: 1Ch
Register type: Read/Write
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Not Recommended for New Designs

6.11 Upstream Isochronous Window 2 Control Register

The upstream isochronous window 2 control register allows software to identify the TC associated with upstream transactions targeting memory addresses in the range defined by the window. See Table 6–6 for a complete description of the register contents.

Device control memory window register offset: 20h
Register type: Read-only, Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6–6. Upstream Isochronous Window 2 Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	RSVD	R	Reserved. Returns 000h when read.
3:1	TC_ID	RW	Traffic class ID. ID of the traffic class that upstream transactions targeting the range defined by the associated window must be mapped to. The default value for this field is 000b.
0	ISOC_WINDOW_EN	RW	Isochronous window enable. 0 = Address window does not impact upstream traffic (default) 1 = Upstream transactions targeting addresses within the range of this window are applied to the appropriate TC

6.12 Upstream Isochronous Window 2 Base Address Register

The upstream isochronous window 2 base address register allows software to configure the base address for this upstream isochronous window. The entire 32-bit field is read/write and acts as scratchpad space if the window is disabled.

Device control memory window register offset: 24h
Register type: Read/Write
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.13 Upstream Isochronous Window 2 Limit Register

The upstream isochronous window 2 limit register allows software to configure the upper address bound for this upstream isochronous window. The entire 32-bit field is read/write and acts as scratchpad space if the window is disabled.

Device control memory window register offset: 28h
Register type: Read/Write
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Not Recommended for New Designs

6.14 Upstream Isochronous Window 3 Control Register

The upstream isochronous window 3 control register allows software to identify the TC associated with upstream transactions targeting memory addresses in the range defined by the window. See Table 6–7 for a complete description of the register contents.

Device control memory window register offset: 2Ch
Register type: Read-only, Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6–7. Upstream Isochronous Window 3 Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:4	RSVD	R	Reserved. Return 000h when read.
3:1	TC_ID	RW	Traffic class ID. ID of the traffic class that upstream transactions targeting the range defined by the associated window must be mapped to. The default value for this field is 000b.
0	ISOC_WINDOW_EN	RW	Isochronous window enable. 0 = Address window does not impact upstream traffic (default) 1 = Upstream transactions targeting addresses within the range of this window are applied to the appropriate TC

6.15 Upstream Isochronous Window 3 Base Address Register

The upstream isochronous window 3 base address register allows software to configure the base address for this upstream isochronous window. The entire 32-bit field is read/write and acts as scratchpad space if the window is disabled.

Device control memory window register offset: 30h
Register type: Read/Write
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.16 Upstream Isochronous Window 3 Limit Register

The upstream isochronous window 3 limit register allows software to configure the upper address bound for this upstream isochronous window. The entire 32-bit field is read/write and acts as scratchpad space if the window is disabled.

Device control memory window register offset: 34h
Register type: Read/Write
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Not Recommended for New Designs

6.17 GPIO Control Register

This register controls the direction of the eight GPIO terminals. This register has no effect on the behavior of GPIO terminals that are enabled to perform secondary functions. The secondary functions share GPIO4 (SCL) and GPIO5 (SDA). This register is an alias of the GPIO control register in the classic PCI configuration space(offset B4h, see Section 4.59). See Table 6–8 for a complete description of the register contents.

Device control memory window register offset: 40h
Register type: Read-only, Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6–8. GPIO Control Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:8	RSVD	R	Reserved. Returns 00h when read.
7†	GPIO7_DIR	RW	GPIO 7 data direction. This bit selects whether GPIO7 is in input or output mode. 0 = Input (default) 1 = Output
6†	GPIO6_DIR	RW	GPIO 6 data direction. This bit selects whether GPIO6 is in input or output mode. 0 = Input (default) 1 = Output
5†	GPIO5_DIR	RW	GPIO 5 data direction. This bit selects whether GPIO5 is in input or output mode. 0 = Input (default) 1 = Output
4†	GPIO4_DIR	RW	GPIO 4 data direction. This bit selects whether GPIO4 is in input or output mode. 0 = Input (default) 1 = Output
3†	GPIO3_DIR	RW	GPIO 3 data direction. This bit selects whether GPIO3 is in input or output mode. 0 = Input (default) 1 = Output
2†	GPIO2_DIR	RW	GPIO 2 data direction. This bit selects whether GPIO2 is in input or output mode. 0 = Input (default) 1 = Output
1†	GPIO1_DIR	RW	GPIO 1 data direction. This bit selects whether GPIO1 is in input or output mode. 0 = Input (default) 1 = Output
0†	GPIO0_DIR	RW	GPIO 0 data direction. This bit selects whether GPIO0 is in input or output mode. 0 = Input (default) 1 = Output

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Not Recommended for New Designs

6.18 GPIO Data Register

This register reads the state of the input mode GPIO terminals and changes the state of the output mode GPIO terminals. Writing to a bit that is in input mode or is enabled for a secondary function is ignored. The secondary functions share GPIO4 (SCL) and GPIO5 (SDA). The default value at power up depends on the state of the GPIO terminals as they default to general-purpose inputs. This register is an alias of the GPIO data register in the classic PCI configuration space (offset B6h, see Section 4.60). See Table 6–9 for a complete description of the register contents.

Device control memory window register offset: 42h
Register type: Read-only, Read/Write
Default value: 00XXh

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

Table 6–9. GPIO Data Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
15:8	RSVD	R	Reserved
7†	GPIO7_Data	RW	GPIO 7 data. This bit reads the state of GPIO7 when in input mode or changes the state of GPIO7 when in output mode.
6†	GPIO6_Data	RW	GPIO 6 data. This bit reads the state of GPIO6 when in input mode or changes the state of GPIO6 when in output mode.
5†	GPIO5_Data	RW	GPIO 5 data. This bit reads the state of GPIO5 when in input mode or changes the state of GPIO5 when in output mode.
4†	GPIO4_Data	RW	GPIO 4 data. This bit reads the state of GPIO4 when in input mode or changes the state of GPIO4 when in output mode.
3†	GPIO3_Data	RW	GPIO 3 data. This bit reads the state of GPIO3 when in input mode or changes the state of GPIO3 when in output mode.
2†	GPIO2_Data	RW	GPIO 2 data. This bit reads the state of GPIO2 when in input mode or changes the state of GPIO2 when in output mode.
1†	GPIO1_Data	RW	GPIO 1 data. This bit reads the state of GPIO1 when in input mode or changes the state of GPIO1 when in output mode.
0†	GPIO0_Data	RW	GPIO 0 data. This bit reads the state of GPIO0 when in input mode or changes the state of GPIO0 when in output mode.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

6.19 Serial-Bus Data Register

The serial-bus data register reads and writes data on the serial-bus interface. Write data is loaded into this register prior to writing the serial-bus slave address register that initiates the bus cycle. When reading data from the serial bus, this register contains the data read after bit 5 (REQBUSY) in the serial-bus control and status register (offset 47h, see Section 6.22) is cleared. This register is an alias for the serial-bus data register in the PCI header (offset B0h, see Section 4.55). This register is reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Device control memory window register offset: 44h
Register type: Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Not Recommended for New Designs

6.20 Serial-Bus Word Address Register

The value written to the serial-bus word address register represents the word address of the byte being read from or written to on the serial-bus interface. The word address is loaded into this register prior to writing the serial-bus slave address register that initiates the bus cycle. This register is an alias for the serial-bus word address register in the PCI header (offset B1h, see Section 4.56). This register is reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Device control memory window register offset: 45h
Register type: Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

6.21 Serial-Bus Slave Address Register

The serial-bus slave address register indicates the address of the device being targeted by the serial-bus cycle. This register also indicates if the cycle will be a read or a write cycle. Writing to this register initiates the cycle on the serial interface. This register is an alias for the serial-bus slave address register in the PCI header (offset B2h, see Section 4.57). See Table 6–10 for a complete description of the register contents.

Device control memory window register offset: 46h
Register type: Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 6–10. Serial-Bus Slave Address Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7:1†	SLAVE_ADDR	RW	Serial-bus slave address. This 7-bit field is the slave address for a serial-bus read or write transaction. The default value for this field is 000 0000b.
0†	RW_CMD	RW	Read/write command. This bit determines if the serial-bus cycle is a read or a write cycle. 0 = A single byte write is requested (default) 1 = A single byte read is requested

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Not Recommended for New Designs

6.22 Serial-Bus Control and Status Register

The serial-bus control and status register controls the behavior of the serial-bus interface. This register also provides status information about the state of the serial-bus. This register is an alias for the serial-bus control and status register in the PCI header (offset B3h, see Section 4.58). See Table 6–11 for a complete description of the register contents.

Device control memory window register offset: 47h
Register type: Read-only, Read/Write, Read/Clear
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

Table 6–11. Serial-Bus Control and Status Register Description

BIT	FIELD NAME	ACCESS	DESCRIPTION
7†	PROT_SEL	RW	Protocol select. This bit selects the serial-bus address mode used. 0 = Slave address and word address are sent on the serial-bus (default) 1 = Only the slave address is sent on the serial-bus
6	RSVD	R	Reserved. Returns 0b when read.
5†	REQBUSY	RU	Requested serial-bus access busy. This bit is set when a software-initiated serial-bus cycle is in progress. 0 = No serial-bus cycle 1 = Serial-bus cycle in progress
4†	ROMBUSY	RU	Serial EEPROM access busy. This bit is set when the serial EEPROM circuitry in the bridge is downloading register defaults from a serial EEPROM. 0 = No EEPROM activity 1 = EEPROM download in progress
3†	SBDETECT	RWU	Serial EEPROM detected. This bit enables the serial-bus interface. The value of this bit controls whether the GPIO4//SCL and GPIO5//SDA terminals are configured as GPIO signals or as serial-bus signals. This bit is automatically set to 1b when a serial EEPROM is detected. **Note:** A serial EEPROM is only detected once following $\overline{\text{PERST}}$. 0 = No EEPROM present, EEPROM load process does not happen. GPIO4//SCL and GPIO5//SDA terminals are configured as GPIO signals. 1 = EEPROM present, EEPROM load process takes place. GPIO4//SCL and GPIO5//SDA terminals are configured as serial-bus signals.
2†	SBTEST	RW	Serial-bus test. This bit is used for internal test purposes. This bit controls the clock source for the serial interface clock. 0 = Serial-bus clock at normal operating frequency ~ 60 kHz (default) 1 = Serial-bus clock frequency increased for test purposes ~ 4 MHz
1†	SB_ERR	RCU	Serial-bus error. This bit is set when an error occurs during a software-initiated serial-bus cycle. 0 = No error 1 = Serial-bus error
0†	ROM_ERR	RCU	Serial EEPROM load error. This bit is set when an error occurs while downloading registers from a serial EEPROM. 0 = No error 1 = EEPROM load error

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Not Recommended for New Designs

6.23 TI Proprietary Register

This read/write TI proprietary register is located at offset 48h and controls TI proprietary functions. This register must not be changed from the specified default state. This register is reset by a PCI Express reset ($\overline{PERST}$), a $\overline{GRST}$, or the internally-generated power-on reset.

Device control memory window register offset: 48h
Register type: Read-only, Read/Write
Default value: 00h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0

6.24 TI Proprietary Register

This read/write TI proprietary register is located at offset 4Ah and controls TI proprietary functions. This register must not be changed from the specified default state. This register is reset by a PCI Express reset ($\overline{PERST}$), a $\overline{GRST}$, or the internally-generated power-on reset.

Device control memory window register offset: 4Ah
Register type: Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.25 TI Proprietary Register

This read/write TI proprietary register is located at offset 4Ch and controls TI proprietary functions. This register must not be changed from the specified default state.

Device control memory window register offset: 4Ch
Register type: Read/Clear
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Not Recommended for New Designs

7 1394 OHCI—PCI Configuration Space

The 1394 OHCI core is integrated as a PCI device behind the PCI-Express to PCI Bridge. The configuration header for the 1394 OHCI portion of the design is compliant with the *PCI Specification* as a standard header. Table 7–1 illustrates the configuration header that includes both the predefined portion of the configuration space and the user definable registers.

Since the 1394 OHCI configuration space is accessed over the bridge secondary PCI bus, PCI Express type 1 configuration read and write transactions are required when accessing these registers. The 1394 OHCI configuration register map is accessed as device number 0 and function number 0. Of course, the bus number is determined by the value that is loaded into the Secondary Bus Number field at offset 19h within the PCI Express configuration register map.

All bits marked with a † are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset. The remaining register bits are reset by a PCI Express hot reset, $\overline{\text{PERST}}$, $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Table 7–1. 1394 OHCI Configuration Register Map

REGISTER NAME				OFFSET
Device ID		Vendor ID		00h
Status		Command		04h
Class code			Revision ID	08h
BIST	Header type	Latency timer	Cache line size	0Ch
OHCI base address				10h
TI extension base address				14h
CIS base address				18h
Reserved				1Ch–27h
CIS pointer				28h
Subsystem ID†		Subsystem vendor ID†		2Ch
Reserved				30h
Reserved			PCI power management capabilities pointer	34h
Reserved				38h
Maximum latency†	Minimum grant†	Interrupt pin	Interrupt line	3Ch
PCI OHCI control				40h
Power management capabilities		Next item pointer	Capability ID	44h
PM data (RSVD)	PMCSR_BSE	Power management control and status†		48h
Reserved				4Ch–EBh
PCI PHY control†				ECh
Miscellaneous configuration†				F0h
Link enhancement control†				F4h
Subsystem access†				F8h
TI proprietary				FCh

† One or more bits in this register are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

7.1 Vendor ID Register

The vendor ID register contains a value allocated by the PCI SIG and identifies the manufacturer of the OHCI controller. The vendor ID assigned to Texas Instruments is 104Ch.

PCI register offset: 00h
Register type: Read-only
Default value: 104Ch

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	1	0	0	0	0	0	1	0	0	1	1	0	0

Not Recommended for New Designs

7.2 Device ID Register

The device ID register contains a value assigned to the 1394 OHCI function by Texas Instruments. The device identification for the 1394 OHCI function is 8235h.

PCI register offset: 02h
Register type: Read-only
Default value: 8235h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	1	0	0	0	0	0	1	0	0	0	1	1	0	1	0	1

7.3 Command Register

The command register provides control over the OHCI controller interface to the PCI bus. All bit functions adhere to the definitions in the *PCI Local Bus Specification*, as seen in the following bit descriptions. See Table 7–2 for a complete description of the register contents.

PCI register offset: 04h
Register type: Read/Write, Read-only
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 7–2. Command Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15–11	RSVD	R	Reserved. Bits 15–11 return 0 0000b when read.
10	INT_DISABLE	R	Interrupt disable. When bit 10 is set to 1b, the OHCI controller is disabled from asserting an interrupt. When cleared, the OHCI controller is able to send interrupts normally. This default value for this bit is 0b.
9	FBB_ENB	R	Fast back-to-back enable. The OHCI controller does not generate fast back-to-back transactions; therefore, bit 9 returns 0b when read.
8	SERR_ENB	RW	$\overline{\text{PCI_SERR}}$ enable. When bit 8 is set to 1b, the OHCI controller $\overline{\text{PCI_SERR}}$ driver is enabled. $\overline{\text{PCI_SERR}}$ can be asserted after detecting an address parity error on the PCI bus. The default value for this bit is 0b.
7	STEP_ENB	R	Address/data stepping control. The OHCI controller does not support address/data stepping; therefore, bit 7 is hardwired to 0b.
6	PERR_ENB	RW	Parity error enable. When bit 6 is set to 1b, the OHCI controller is enabled to drive $\overline{\text{PCI_PERR}}$ response to parity errors through the $\overline{\text{PCI_PERR}}$ signal. The default value for this bit is 0b.
5	VGA_ENB	R	VGA palette snoop enable. The OHCI controller does not feature VGA palette snooping; therefore, bit 5 returns 0b when read.
4	MWI_ENB	RW	Memory write and invalidate enable. When bit 4 is set to 1b, the OHCI controller is enabled to generate MWI PCI bus commands. If this bit is cleared, then the OHCI controller generates memory write commands instead. The default value for this bit is 0b.
3	SPECIAL	R	Special cycle enable. The OHCI controller function does not respond to special cycle transactions; therefore, bit 3 returns 0b when read.
2	MASTER_ENB	RW	Bus master enable. When bit 2 is set to 1b, the OHCI controller is enabled to initiate cycles on the PCI bus. The default value for this bit is 0b.
1	MEMORY_ENB	RW	Memory response enable. Setting bit 1 to 1b enables the OHCI controller to respond to memory cycles on the PCI bus. This bit must be set to access OHCI registers. The default value for this bit is 0b.
0	IO_ENB	R	I/O space enable. The OHCI controller does not implement any I/O-mapped functionality; therefore, bit 0 returns 0b when read.

Not Recommended for New Designs

7.4 Status Register

The status register provides status over the OHCI controller interface to the PCI bus. All bit functions adhere to the definitions in the *PCI Local Bus Specification*, as seen in the following bit descriptions. See Table 7–3 for a complete description of the register contents.

PCI register offset: 06h
Register type: Read/Clear/Update, Read-only
Default value: 0230h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0	0

Table 7–3. Status Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15	PAR_ERR	RCU	Detected parity error. Bit 15 is set to 1b when either an address parity or data parity error is detected.
14	SYS_ERR	RCU	Signaled system error. Bit 14 is set to 1b when $\overline{\text{PCI_SERR}}$ is enabled and the OHCI controller has signaled a system error to the host.
13	MABORT	RCU	Received master abort. Bit 13 is set to 1b when a cycle initiated by the OHCI controller on the PCI bus has been terminated by a master abort.
12	TABORT_REC	RCU	Received target abort. Bit 12 is set to 1b when a cycle initiated by the OHCI controller on the PCI bus was terminated by a target abort.
11	TABORT_SIG	RCU	Signaled target abort. Bit 11 is set to 1b by the OHCI controller when it terminates a transaction on the PCI bus with a target abort.
10–9	PCI_SPEED	R	DEVSEL timing. Bits 10 and 9 encode the timing of $\overline{\text{PCI_DEVSEL}}$ and are hardwired to 01b, indicating that the OHCI controller asserts this signal at a medium speed on nonconfiguration cycle accesses.
8	DATAPAR	RCU	Data parity error detected. Bit 8 is set to 1b when the following conditions have been met: a. $\overline{\text{PCI_PERR}}$ was asserted by any PCI device including the OHCI controller. b. The OHCI controller was the bus master during the data parity error. c. Bit 6 (PERR_EN) in the command register at offset 04h in the PCI configuration space (see Section 7.3, *Command Register*) is set to 1b.
7	FBB_CAP	R	Fast back-to-back capable. The OHCI controller cannot accept fast back-to-back transactions; therefore, bit 7 is hardwired to 0b.
6	UDF	R	User-definable features (UDF) supported. The OHCI controller does not support the UDF; therefore, bit 6 is hardwired to 0b.
5	66MHZ	R	66-MHz capable. The OHCI controller operates at a maximum PCI_CLK frequency of 66 MHz; therefore, bit 5 is hardwired to 1b.
4	CAPLIST	R	Capabilities list. Bit 4 returns 1b when read, indicating that capabilities additional to standard PCI are implemented. The linked list of PCI power-management capabilities is implemented in this function.
3	INT_STATUS	RU	Interrupt status. This bit reflects the interrupt status of the function. Only when bit 10 (INT_DISABLE) in the command register (PCI offset 04h, see Section 4.3) is a 0 and this bit is a 1, is the function's $\overline{\text{INTx}}$ signal asserted. Setting the INT_DISABLE bit to a 1 has no effect on the state of this bit. This bit has been defined as part of the *PCI Local Bus Specification* (Revision 2.3).
2–0	RSVD	R	Reserved. Bits 3–0 return 0h when read.

Not Recommended for New Designs

7.5 Class Code and Revision ID Register

The class code and revision ID register categorizes the OHCI controller as a serial bus controller (0Ch), controlling an IEEE 1394 bus (00h), with an OHCI programming model (10h). Furthermore, the TI chip revision is indicated in the least significant byte. See Table 7–4 for a complete description of the register contents.

PCI register offset: 08h
Register type: Read-only
Default value: 0C00 1001h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1

Table 7–4. Class Code and Revision ID Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–24	BASECLASS	R	Base class. This field returns 0Ch when read, which broadly classifies the function as a serial bus controller.
23–16	SUBCLASS	R	Subclass. This field returns 00h when read, which specifically classifies the function as controlling an IEEE 1394 serial bus.
15–8	PGMIF	R	Programming interface. This field returns 10h when read, which indicates that the programming model is compliant with the *1394 Open Host Controller Interface Specification*.
7–0	CHIPREV	R	Silicon revision. This field returns 01h when read, which indicates the silicon revision of the OHCI controller.

7.6 Latency Timer and Class Cache Line Size Register

The latency timer and class cache line size register is programmed by host BIOS to indicate system cache line size and the latency timer associated with the OHCI controller. See Table 7–5 for a complete description of the register contents.

PCI register offset: 0Ch
Register type: Read/Write
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 7–5. Latency Timer and Class Cache Line Size Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15–8	LATENCY_TIMER	RW	PCI latency timer. The value in this register specifies the latency timer for the OHCI controller, in units of PCI clock cycles. When the OHCI controller is a PCI bus initiator and asserts $\overline{\text{FRAME}}$, the latency timer begins counting from 0. If the latency timer expires before the OHCI controller transaction has terminated, then the OHCI controller terminates the transaction when its $\overline{\text{GNT}}$ is deasserted. The default value for this field is 00h.
7–0	CACHELINE_SZ	RW	Cache line size. This value is used by the OHCI controller during memory write and invalidate, memory-read line, and memory-read multiple transactions. The default value for this field is 00h.

Not Recommended for New Designs

7.7 Header Type and BIST Register

The header type and built-in self-test (BIST) register indicates the OHCI controller PCI header type and no built-in self-test. See Table 7–6 for a complete description of the register contents.

PCI register offset: 0Eh
Register type: Read-only
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 7–6. Header Type and BIST Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15–8	BIST	R	Built-in self-test. The OHCI controller does not include a BIST; therefore, this field returns 00h when read.
7–0	HEADER_TYPE	R	PCI header type. The OHCI controller includes the standard PCI header, which is communicated by returning 00h when this field is read. Since the 1394 OHCI core is implemented as a single function PCI device, bit 7 of this register must be 0b.

7.8 OHCI Base Address Register

The OHCI base address register is programmed with a base address referencing the memory-mapped OHCI control. When BIOS writes all 1s to this register, the value read back is FFFF F800h, indicating that at least 2K bytes of memory address space are required for the OHCI registers. See Table 7–7 for a complete description of the register contents.

PCI register offset: 10h
Register type: Read/Write, Read-only
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 7–7. OHCI Base Address Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–11	OHCIREG_PTR	RW	OHCI register pointer. This field specifies the upper 21 bits of the 32-bit OHCI base address register. The default value for this field is all 0s.
10–4	OHCI_SZ	R	OHCI register size. This field returns 000 0000b when read, indicating that the OHCI registers require a 2K-byte region of memory.
3	OHCI_PF	R	OHCI register prefetch. Bit 3 returns 0b when read, indicating that the OHCI registers are nonprefetchable.
2–1	OHCI_MEMTYPE	R	OHCI memory type. This field returns 00b when read, indicating that the OHCI base address register is 32 bits wide and mapping can be done anywhere in the 32-bit memory space.
0	OHCI_MEM	R	OHCI memory indicator. Bit 0 returns 0b when read, indicating that the OHCI registers are mapped into system memory space.

Not Recommended for New Designs

7.9 TI Extension Base Address Register

The TI extension base address register is programmed with a base address referencing the memory-mapped TI extension registers. When BIOS writes all 1s to this register, the value read back is FFFF C000h, indicating that at least 16K bytes of memory address space are required for the TI registers. See Table 7–8 for a complete description of the register contents.

PCI register offset: 14h
Register type: Read/Write, Read-only
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 7–8. TI Base Address Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–14	TIREG_PTR	RW	TI register pointer. This field specifies the upper 18 bits of the 32-bit TI base address register. The default value for this field is all 0s.
13–4	TI_SZ	R	TI register size. This field returns 00 0000 0000b when read, indicating that the TI registers require a 16K-byte region of memory.
3	TI_PF	R	TI register prefetch. Bit 3 returns 0b when read, indicating that the TI registers are nonprefetchable.
2–1	TI_MEMTYPE	R	TI memory type. This field returns 00b when read, indicating that the TI base address register is 32 bits wide and mapping can be done anywhere in the 32-bit memory space.
0	TI_MEM	R	TI memory indicator. Bit 0 returns 0b when read, indicating that the TI registers are mapped into system memory space.

7.10 CIS Base Address Register

The $\overline{\text{CARDBUS}}$ input to the 1394 OHCI core is tied high such that this register returns 0000 0000h when read.

PCI register offset: 18h
Register type: Read-only
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

7.11 CIS Pointer Register

The $\overline{\text{CARDBUS}}$ input to the 1394 OHCI core is tied high such that this register returns 0000 0000h when read.

PCI register offset: 28h
Register type: Read-only
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Not Recommended for New Designs

7.12 Subsystem Identification Register

The subsystem identification register is used for system and option card identification purposes. This register can be initialized from the serial EEPROM or programmed via the subsystem access register at offset F8h in the PCI configuration space (see Section 7.24, *Subsystem Access Register*). See Table 7–9 for a complete description of the register contents.

PCI register offset: 2Ch
Register type: Read/Update
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 7–9. Subsystem Identification Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–16†	OHCI_SSID	RU	Subsystem device ID. This field indicates the subsystem device ID.
15–0†	OHCI_SSVID	RU	Subsystem vendor ID. This field indicates the subsystem vendor ID.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

7.13 Power Management Capabilities Pointer Register

The power management capabilities pointer register provides a pointer into the PCI configuration header where the power-management register block resides. The OHCI controller configuration header doublewords at offsets 44h and 48h provide the power-management registers. This register is read-only and returns 44h when read.

PCI register offset: 34h
Register type: Read-only
Default value: 44h

BIT NUMBER	7	6	5	4	3	2	1	0
RESET STATE	0	1	0	0	0	1	0	0

7.14 Interrupt Line and Pin Register

The interrupt line and pin register communicates interrupt line routing information. See Table 7–10 for a complete description of the register contents.

PCI register offset: 3Ch
Register type: Read/Write
Default value: 0100h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Table 7–10. Interrupt Line and Pin Registers Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15–8	INTR_PIN	R	Interrupt pin. This field returns 01h when read, indicating that the 1394 OHCI core signals interrupts on the $\overline{\text{INTA}}$ terminal.
7–0	INTR_LINE	RW	Interrupt line. This field is programmed by the system and indicates to software which interrupt line the OHCI controller $\overline{\text{INTA}}$ is connected to. The default value for this field is all 00h.

Not Recommended for New Designs

7.15 MIN_GNT and MAX_LAT Register

The MIN_GNT and MAX_LAT register communicates to the system the desired setting of bits 15–8 in the latency timer and class cache line size register at offset 0Ch in the PCI configuration space (see Section 7.6, *Latency Timer and Class Cache Line Size Register*). If a serial EEPROM is detected, then the contents of this register are loaded through the serial EEPROM interface. If no serial EEPROM is detected, then this register returns a default value that corresponds to the MAX_LAT = 4, MIN_GNT = 2. See Table 7–11 for a complete description of the register contents.

PCI register offset: 3Eh
Register type: Read/Update
Default value: 0402h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0

Table 7–11. MIN_GNT and MAX_LAT Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15–8†	MAX_LAT	RU	Maximum latency. The contents of this field may be used by host BIOS to assign an arbitration priority level to the OHCI controller. The default for this register indicates that the OHCI controller may need to access the PCI bus as often as every 0.25 µs; thus, an extremely high priority level is requested. Bits 11–8 of this field may also be loaded through the serial EEPROM.
7–0†	MIN_GNT	RU	Minimum grant. The contents of this field may be used by host BIOS to assign a latency timer register value to the OHCI controller. The default for this register indicates that the OHCI controller may need to sustain burst transfers for nearly 64 µs and thus request a large value be programmed in bits 15–8 of the OHCI controller latency timer and class cache line size register at offset 0Ch in the PCI configuration space (see Section 7.6, *Latency Timer and Class Cache Line Size Register*). Bits 3–0 of this field may also be loaded through the serial EEPROM.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

7.16 OHCI Control Register

The PCI OHCI control register is defined by the *1394 Open Host Controller Interface Specification* and provides a bit for big endian PCI support. See Table 7–12 for a complete description of the register contents.

PCI register offset: 40h
Register type: Read/Write, Read-only
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 7–12. OHCI Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–1	RSVD	R	Reserved. Bits 31–1 return 000 0000 0000 0000 0000 0000 0000 0000b when read.
0	GLOBAL_SWAP	RW	When bit 0 is set to 1b, all quadlets read from and written to the PCI interface are byte-swapped (big endian). The default value for this bit is 0b which is little endian mode.

Not Recommended for New Designs

7.17 Capability ID and Next Item Pointer Registers

The capability ID and next item pointer register identifies the linked-list capability item and provides a pointer to the next capability item. See Table 7–13 for a complete description of the register contents.

PCI register offset: 44h
Register type: Read-only
Default value: 0001h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Table 7–13. Capability ID and Next Item Pointer Registers Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15–8	NEXT_ITEM	R	Next item pointer. The OHCI controller supports only one additional capability that is communicated to the system through the extended capabilities list; therefore, this field returns 00h when read.
7–0	CAPABILITY_ID	R	Capability identification. This field returns 01h when read, which is the unique ID assigned by the PCI SIG for PCI power-management capability.

7.18 Power Management Capabilities Register

The power management capabilities register indicates the capabilities of the OHCI core related to PCI power management. See Table 7–14 for a complete description of the register contents.

PCI register offset: 46h
Register type: Read-only
Default value: 7E02h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	1	1	1	1	1	1	0	0	0	0	0	0	0	1	0

Table 7–14. Power Management Capabilities Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15–11	PME_SUPPORT	R	$\overline{PME}$ support. This 5-bit field indicates the power states from which the OHCI core may assert $\overline{PME}$. This field returns a value of 01111b, indicating that $\overline{PME}$ is asserted from the $D3_{hot}$, D2, D1, and D0 power states.
10	D2_SUPPORT	R	D2 support. Bit 10 is hardwired to 1b, indicating that the OHCI controller supports the D2 power state.
9	D1_SUPPORT	R	D1 support. Bit 9 is hardwired to 1b, indicating that the OHCI controller supports the D1 power state.
8–6	AUX_CURRENT	R	Auxiliary current. This 3-bit field reports the 3.3-V_{AUX} auxiliary current requirements. This field returns 000b, because the 1394a core is not powered by V_{AUX}.
5	DSI	R	Device-specific initialization. This bit returns 0b when read, indicating that the OHCI controller does not require special initialization beyond the standard PCI configuration header before a generic class driver is able to use it.
4	RSVD	R	Reserved. Bit 4 returns 0b when read.
3	PME_CLK	R	$\overline{PME}$ clock. This bit returns 0b when read, indicating that no host bus clock is required for the OHCI controller to generate $\overline{PME}$.
2–0	PM_VERSION	R	Power-management version. If bit 7 (PCI_PM_VERSION_CTRL) in the PCI miscellaneous configuration register at offset F0h (see Section 7.22) is 0b, then this field returns 010b indicating Revision 1.1 compatibility. If PCI_PM_VERSION_CTRL in the PCI miscellaneous configuration register is 1b, then this field returns 011b indicating Revision 1.2 compatibility.

Not Recommended for New Designs

7.19 Power Management Control and Status Register

The power management control and status register implements the control and status of the PCI power management function. This register is not affected by the internally-generated reset caused by the transition from the $D3_{hot}$ to D0 state. See Table 7–15 for a complete description of the register contents.

PCI register offset: 48h
Register type: Read/Write, Read-only
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 7–15. Power Management Control and Status Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15	PME_STS	R	This bit returns 0b, because $\overline{PME}$ is not supported.
14–13	DATA_SCALE	R	This field returns 00b, because the data register is not implemented.
12–9	DATA_SELECT	R	This field returns 0h, because the data register is not implemented.
8	PME_ENB	R	This bit returns 0b, because $\overline{PME}$ is not supported.
7–2	RSVD	R	Reserved. Bits 7–2 return 00 0000b when read.
1–0†	PWR_STATE	RW	Power state. This 2-bit field sets the OHCI controller power state and is encoded as follows: 00 = Current power state is D0 (default) 01 = Current power state is D1 10 = Current power state is D2 11 = Current power state is D3

† These bits are reset on the rising edge of PCI bus reset ($\overline{PRST}$).

7.20 Power Management Extension Registers

The power management extension register provides extended power-management features not applicable to the OHCI controller; thus, it is read-only and returns 0000h when read. See Table 7–16 for a complete description of the register contents.

PCI register offset: 4Ah
Register type: Read-only
Default value: 0000h

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 7–16. Power Management Extension Registers Description

BIT	FIELD NAME	TYPE	DESCRIPTION
15–0	RSVD	R	Reserved. Bits 15–0 return 0000h when read.

Not Recommended for New Designs

7.21 PCI PHY Control Register

The PCI PHY control register provides a method for enabling the PHY CNA output. See Table 7–17 for a complete description of the register contents.

PCI register offset: ECh
Register type: Read/Write, Read-only
Default value: 0000 0008h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Table 7–17. PCI PHY Control Register

BIT	FIELD NAME	TYPE	DESCRIPTION
31–8	RSVD	R	Reserved. Bits 31–8 return 00 0000h when read.
7†	CNAOUT	RW	When bit 7 is set to 1b, the PHY CNA output is routed to terminal U09. When implementing a serial EEPROM, this bit can be set by programming bit 7 of offset 38h in the EEPROM to 1.
6–5	RSVD	R	Reserved. Bits 6–5 return 00b when read.
4†	RSVD	RW	Reserved. Bit 4 defaults to 0b and must remain 0b for normal operation of the PHY.
3†	RSVD	RW	Reserved. Bit 3 defaults to 1b to indicate compliance with IEEE Std 1394a-2000. If a serial EEPROM is implemented, then bit 3 at EEPROM byte offset 38h must be set to 1. See Table 3–10, *EEPROM Register Loading Map*.
2†	RSVD	RW	Reserved. Bit 2 defaults to 0b and must remain 0b for normal operation of the PHY.
1†	RSVD	RW	Reserved. Bit 1 defaults to 0b and must remain 0b for normal operation of the PHY. If a serial EEPROM is implemented, then bit 1 at EEPROM byte offset 38h must be set to 0. See Table 3–10, *EEPROM Register Loading Map*.
0†	RSVD	RW	Reserved. Bit 0 defaults to 0b and must remain 0b for normal operation of the PHY.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Not Recommended for New Designs

7.22 PCI Miscellaneous Configuration Register

The PCI miscellaneous configuration register provides miscellaneous PCI-related configuration. See Table 7–18 for a complete description of the register contents.

PCI register offset: F0h
Register type: Read/Write, Read-only
Default value: 0000 0800h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Table 7–18. Miscellaneous Configuration Register

BIT	FIELD NAME	TYPE	DESCRIPTION
31–16	RSVD	R	Reserved. Bits 31–16 return 0000h when read.
15	PME_D3COLD	R	$\overline{PME}$ support from $D3_{cold}$. The 1394a OHCI core does not support PME generation from $D3_{cold}$. Therefore, this bit is tied to 0b.
14–12	RSVD	R	Reserved. Bits 14–12 return 000b when read.
11	PCI2_3_EN	R	PCI 2.3 enable. The 1394 OHCI core always conforms to the PCI 2.3 specification; therefore, this bit is tied to 1b.
10	IGNORE_ MSTRINT_ ENA_FOR_PME	RW	IGNORE_MSTRINT_ENA_FOR_PME bit for $\overline{PME}$ generation. When set, this bit causes bit 26 of the OHCI vendor ID register (OHCI offset 40h, see Section 8.15) to read 1b. Otherwise, bit 26 reads 0b. 0 = $\overline{PME}$ behavior generated from unmasked interrupt bits and IntMask.masterIntEnable bit (default) 1 = $\overline{PME}$ generation does not depend on the value of IntMask.masterIntEnable
9–8†	MR_ENHANCE	RW	This field selects the read command behavior of the PCI master for read transactions of greater than two data phases. For read transactions of one or two data phases, a memory read command is used. 00 = Memory read line (default) 01 = Memory read 10 = Memory read multiple 11 = Reserved, behavior reverts to default
7†	PCI_PM_ VERSION_CTRL	RW	PCI power management version control. This bit controls the value reported in the Version field of the power management capabilities register of the 1394 OHCI function. 0 = Version fields report 010b for Power Management 1.1 compliance (default) 1 = Version fields report 011b for Power Management 1.2 compliance
6–5	RSVD	R	Reserved. Bits 6–5 return 00b when read.
4†	DIS_TGT_ABT	RW	Disable target abort. Bit 4 controls the no-target-abort mode, in which the OHCI controller returns indeterminate data instead of signaling target abort. The OHCI LLC is divided into the PCLK and SCLK domains. If software tries to access registers in the link that are not active because the SCLK is disabled, then a target abort is issued by the link. On some systems, this can cause a problem resulting in a fatal system error. Enabling this bit allows the link to respond to these types of requests by returning FFh. 0 = Responds with OHCI-Lynx™ compatible target abort (default) 1 = Responds with indeterminate data equal to FFh. It is recommended that this bit be set to 1b
3†	SB_EN	RW	Serial bus enable. In the bridge, the serial bus interface is controlled using the bridge configuration registers. Therefore, this bit has no effect in the 1394a OHCI function. The default value for this bit is 0b.
2†	DISABLE_ SCLKGATE	RW	Disable SCLK test feature. This bit controls locking or unlocking the SCLK to the 1394a OHCI core PCI bus clock input. This is a test feature only and must be cleared to 0b (all applications). 0 = Hardware decides auto-gating of the PHY clock (default) 1 = Disables auto-gating of the PHY clock

† These bits are reset by a PCI Express reset ($\overline{PERST}$), a $\overline{GRST}$, or the internally-generated power-on reset.

Not Recommended for New Designs

Table 7–18. Miscellaneous Configuration Register (Continued)

BIT	FIELD NAME	TYPE	DESCRIPTION
1†	DISABLE_PCIGATE	RW	Disable PCLK test feature. This bit controls locking or unlocking the PCI clock to the 1394a OHCI core PCI bus clock input. This is a test feature only and must be cleared to 0b (all applications). 0 = Hardware decides auto-gating of the PCI clock (default) 1 = Disables auto-gating of the PCI clock
0†	KEEP_PCLK	RW	Keep PCI clock running. This bit controls the PCI clock operation during the CLKRUN protocol. Since the CLKRUN protocol is not supported in the XIO2200A, this bit has no effect. The default value for this bit is 0b.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

7.23 Link Enhancement Control Register

The link enhancement control register implements TI proprietary bits that are initialized by software or by a serial EEPROM, if present. After these bits are set to 1b, their functionality is enabled only if bit 22 (aPhyEnhanceEnable) in the host controller control register at OHCI offset 50h/54h (see Section 8.16, *Host Controller Control Register*) is set to 1. See Table 7–19 for a complete description of the register contents.

PCI register offset: F4h
Register type: Read/Write, Read-only
Default value: 0000 1000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Table 7–19. Link Enhancement Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–16	RSVD	R	Reserved. Bits 31–16 return 0000h when read.
15†	dis_at_pipeline	RW	Disable AT pipelining. When bit 15 is set to 1b, out-of-order AT pipelining is disabled. The default value for this bit is 0b.
14†	RSVD	RW	Reserved. Bit 14 defaults to 0b and must remain 0b for normal operation of the OHCI core.
13–12†	atx_thresh	RW	This field sets the initial AT threshold value, which is used until the AT FIFO is underrun. When the OHCI controller retries the packet, it uses a 2K-byte threshold, resulting in a store-and-forward operation. 00 = Threshold ~ 2K bytes resulting in a store-and-forward operation 01 = Threshold ~ 1.7K bytes (default) 10 = Threshold ~ 1K bytes 11 = Threshold ~ 512 bytes These bits fine-tune the asynchronous transmit threshold. For most applications the 1.7K-byte threshold is optimal. Changing this value may increase or decrease the 1394 latency depending on the average PCI bus latency. Setting the AT threshold to 1.7K, 1K, or 512 bytes results in data being transmitted at these thresholds or when an entire packet has been checked into the FIFO. If the packet to be transmitted is larger than the AT threshold, then the remaining data must be received before the AT FIFO is emptied; otherwise, an underrun condition occurs, resulting in a packet error at the receiving node. As a result, the link then commences store-and-forward operation. Wait until it has the complete packet in the FIFO before retransmitting it on the second attempt to ensure delivery. An AT threshold of 2K results in store-and-forward operation, which means that asynchronous data will not be transmitted until an end-of-packet token is received. Restated, setting the AT threshold to 2K results in only complete packets being transmitted. Note that the OHCI controller will always use store-and-forward when the asynchronous transmit retries register at OHCI offset 08h (see Section 8.3, *Asynchronous Transmit Retries Register*) is cleared.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Not Recommended for New Designs

Table 7–19. Link Enhancement Control Register Description (Continued)

BIT	FIELD NAME	TYPE	DESCRIPTION
11	RSVD	R	Reserved. Bit 11 returns 0b when read.
10†	enab_mpeg_ts	RW	Enable MPEG CIP timestamp enhancement. When bit 9 is set to 1b, the enhancement is enabled for MPEG CIP transmit streams (FMT = 20h). The default value for this bit is 0b.
9	RSVD	R	Reserved. Bit 9 returns 0b when read.
8†	enab_dv_ts	RW	Enable DV CIP timestamp enhancement. When bit 8 is set to 1b, the enhancement is enabled for DV CIP transmit streams (FMT = 00h). The default value for this bit is 0b.
7†	enab_unfair	RW	Enable asynchronous priority requests. OHCI-Lynx™ compatible. Setting bit 7 to 1b enables the link to respond to requests with priority arbitration. It is recommended that this bit be set to 1b. The default value for this bit is 0b.
6–3	RSVD	R	Reserved. Bits 6–3 return 0h when read.
2†	RSVD	RW	Reserved. Bit 2 defaults to 0b and must remain 0b for normal operation of the OHCI core.
1†	enab_accel	RW	Enable acceleration enhancements. OHCI-Lynx™ compatible. When bit 1 is set to 1b, the PHY layer is notified that the link supports the IEEE Std 1394a-2000 acceleration enhancements, that is, ack-accelerated, fly-by concatenation, etc. It is recommended that this bit be set to 1b. The default value for this bit is 0b.
0	RSVD	R	Reserved. Bit 0 returns 0b when read.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

7.24 Subsystem Access Register

Write access to the subsystem access register updates the subsystem identification registers identically to OHCI-Lynx™. The system ID value written to this register may also be read back from this register. See Table 7–20 for a complete description of the register contents.

PCI register offset: F8h
Register type: Read/Write
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 7–20. Subsystem Access Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–16†	SUBDEV_ID	RW	Subsystem device ID alias. This field indicates the subsystem device ID.
15–0†	SUBVEN_ID	RW	Subsystem vendor ID alias. This field indicates the subsystem vendor ID.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

7.25 TI Proprietary Register

This read-only TI proprietary register is located at offset E2h. The default state is 0000 0000h.

PCI register offset: FCh
Register type: Read-only
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Not Recommended for New Designs

8 1394 OHCI Memory-Mapped Register Space

The OHCI registers defined by the *1394 Open Host Controller Interface Specification* are memory-mapped into a 2K-byte region of memory pointed to by the OHCI base address register at offset 10h in PCI configuration space (see Section 7.8). These registers are the primary interface for controlling the IEEE 1394 link function.

This section provides the register interface and bit descriptions. Several set/clear register pairs in this programming model are implemented to solve various issues with typical read-modify-write control registers. There are two addresses for a set/clear register: RegisterSet and RegisterClear. See Table 8–1 for a register listing. A 1 bit written to RegisterSet causes the corresponding bit in the set/clear register to be set to 1b; a 0 bit leaves the corresponding bit unaffected. A 1 bit written to RegisterClear causes the corresponding bit in the set/clear register to be cleared; a 0 bit leaves the corresponding bit in the set/clear register unaffected.

Typically, a read from either RegisterSet or RegisterClear returns the contents of the set or clear register, respectively. However, sometimes reading the RegisterClear provides a masked version of the set or clear register. The interrupt event register is an example of this behavior.

Table 8–1. OHCI Register Map

DMA CONTEXT	REGISTER NAME	ABBREVIATION	OFFSET
—	OHCI version	Version	00h
	GUID ROM	GUID_ROM	04h
	Asynchronous transmit retries	ATRetries	08h
	CSR data	CSRData	0Ch
	CSR compare	CSRCompareData	10h
	CSR control	CSRControl	14h
	Configuration ROM header	ConfigROMhdr	18h
	Bus identification	BusID	1Ch
	Bus options †	BusOptions	20h
	GUID high †	GUIDHi	24h
	GUID low †	GUIDLo	28h
	Reserved	—	2Ch–30h
	Configuration ROM mapping	ConfigROMmap	34h
	Posted write address low	PostedWriteAddressLo	38h
	Posted write address high	PostedWriteAddressHi	3Ch
	Vendor ID	VendorID	40h
	Reserved	—	44h–4Ch
	Host controller control †	HCControlSet	50h
		HCControlClr	54h
	Reserved	—	58h–5Ch
Self-ID	Reserved	—	60h
	Self-ID buffer pointer	SelfIDBuffer	64h
	Self-ID count	SelfIDCount	68h
	Reserved	—	6Ch
—	Isochronous receive channel mask high	IRChannelMaskHiSet	70h
		IRChannelMaskHiClear	74h
	Isochronous receive channel mask low	IRChannelMaskLoSet	78h
		IRChannelMaskLoClear	7Ch

† One or more bits in this register are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Not Recommended for New Designs

Table 8–1. OHCI Register Map (Continued)

DMA CONTEXT	REGISTER NAME	ABBREVIATION	OFFSET
—	Interrupt event	IntEventSet	80h
		IntEventClear	84h
	Interrupt mask	IntMaskSet	88h
		IntMaskClear	8Ch
	Isochronous transmit interrupt event	IsoXmitIntEventSet	90h
		IsoXmitIntEventClear	94h
	Isochronous transmit interrupt mask	IsoXmitIntMaskSet	98h
		IsoXmitIntMaskClear	9Ch
—	Isochronous receive interrupt event	IsoRecvIntEventSet	A0h
		IsoRecvIntEventClear	A4h
	Isochronous receive interrupt mask	IsoRecvIntMaskSet	A8h
		IsoRecvIntMaskClear	ACh
	Initial bandwidth available	InitialBandwidthAvailable	B0h
	Initial channels available high	InitialChannelsAvailableHi	B4h
	Initial channels available low	InitialChannelsAvailableLo	B8h
	Reserved	—	BCh–D8h
	Fairness control	FairnessControl	DCh
	Link control †	LinkControlSet	E0h
		LinkControlClear	E4h
	Node identification	NodeID	E8h
	PHY layer control	PhyControl	ECh
	Isochronous cycle timer	Isocyctimer	F0h
	Reserved	—	F4h–FCh
	Asynchronous request filter high	AsyncRequestFilterHiSet	100h
		AsyncRequestFilterHiClear	104h
	Asynchronous request filter low	AsyncRequestFilterLoSet	108h
		AsyncRequestFilterLoClear	10Ch
	Physical request filter high	PhysicalRequestFilterHiSet	110h
		PhysicalRequestFilterHiClear	114h
	Physical request filter low	PhysicalRequestFilterLoSet	118h
		PhysicalRequestFilterLoClear	11Ch
	Physical upper bound	PhysicalUpperBound	120h
	Reserved	—	124h–17Ch
Asynchronous Request Transmit [ATRQ]	Asynchronous context control	ContextControlSet	180h
		ContextControlClear	184h
	Reserved	—	188h
	Asynchronous context command pointer	CommandPtr	18Ch
	Reserved	—	190h–19Ch
Asynchronous Response Transmit [ATRS]	Asynchronous context control	ContextControlSet	1A0h
		ContextControlClear	1A4h
	Reserved	—	1A8h
	Asynchronous context command pointer	CommandPtr	1ACh
	Reserved	—	1B0h–1BCh

† One or more bits in this register are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Not Recommended for New Designs

Table 8–1. OHCI Register Map (Continued)

DMA CONTEXT	REGISTER NAME	ABBREVIATION	OFFSET
Asynchronous Request Receive [ARRQ]	Asynchronous context control	ContextControlSet	1C0h
		ContextControlClear	1C4h
	Reserved	—	1C8h
	Asynchronous context command pointer	CommandPtr	1CCh
	Reserved	—	1D0h–1DCh
Asynchronous Response Receive [ARRS]	Asynchronous context control	ContextControlSet	1E0h
		ContextControlClear	1E4h
	Reserved	—	1E8h
	Asynchronous context command pointer	CommandPtr	1ECh
	Reserved	—	1F0h–1FCh
Isochronous Transmit Context n n = 0, 1, 2, 3, …, 7	Isochronous transmit context control	ContextControlSet	200h + 16*n
		ContextControlClear	204h + 16*n
	Reserved	—	208h + 16*n
	Isochronous transmit context command pointer	CommandPtr	20Ch + 16*n
	Reserved	—	210h–3FCh
Isochronous Receive Context n n = 0, 1, 2, 3	Isochronous receive context control	ContextControlSet	400h + 32*n
		ContextControlClear	404h + 32*n
	Reserved	—	408h + 32*n
	Isochronous receive context command pointer	CommandPtr	40Ch + 32*n
	Isochronous receive context match	ContextMatch	410h + 32*n

8.1 OHCI Version Register

The OHCI version register indicates the OHCI version support and whether or not the serial EEPROM is present. See Table 8–2 for a complete description of the register contents.

OHCI register offset: 00h
Register type: Read-only
Default value: 0X01 0010h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	X	0	0	0	0	0	0	0	1

BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Table 8–2. OHCI Version Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–25	RSVD	R	Reserved. Bits 31–25 return 000 0000b when read.
24†	GUID_ROM	RU	The controller sets bit 24 to 1b if the serial EEPROM is detected. If the serial EEPROM is present, then the Bus_Info_Block is automatically loaded on system (hardware) reset. The default value for this bit is 0b.
23–16	version	R	Major version of the OHCI. The controller is compliant with the *1394 Open Host Controller Interface Specification* (Release 1.1); thus, this field reads 01h.
15–8	RSVD	R	Reserved. Bits 15–8 return 00h when read.
7–0	revision	R	Minor version of the OHCI. The controller is compliant with the *1394 Open Host Controller Interface Specification* (Release 1.1); thus, this field reads 10h.

† One or more bits in this register are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Not Recommended for New Designs

8.2 GUID ROM Register

The GUID ROM register accesses the serial EEPROM, and is only applicable if bit 24 (GUID_ROM) in the OHCI version register at OHCI offset 00h (see Section 8.1) is set to 1b. See Table 8–3 for a complete description of the register contents.

OHCI register offset: 04h
Register type: Read/Set/Update, Read/Update, Read-only
Default value: 00XX 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 8–3. GUID ROM Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	addrReset	RSU	Software sets bit 31 to 1b to reset the GUID ROM address to 0. When the controller completes the reset, it clears this bit. The controller does not automatically fill bits 23–16 (rdData field) with the 0th byte.
30–26	RSVD	R	Reserved. Bits 30–26 return 00 0000b when read.
25	rdStart	RSU	A read of the currently addressed byte is started when bit 25 is set to 1b. This bit is automatically cleared when the controller completes the read of the currently addressed GUID ROM byte.
24	RSVD	R	Reserved. Bit 24 returns 0b when read.
23–16	rdData	RU	This field contains the data read from the GUID ROM.
15–8	RSVD	R	Reserved. Bits 15–8 return 00h when read.
7–0	miniROM	R	The miniROM field defaults to 00h indicating that no mini-ROM is implemented. If an EEPROM is implemented, then all 8 bits of this miniROM field are downloaded from EEPROM word offset 28h. For this device, the miniROM field must be greater than 39h to indicate a valid miniROM offset into the EEPROM.

Not Recommended for New Designs

8.3 Asynchronous Transmit Retries Register

The asynchronous transmit retries register indicates the number of times the controller attempts a retry for asynchronous DMA request transmit and for asynchronous physical and DMA response transmit. See Table 8–4 for a complete description of the register contents.

OHCI register offset: 08h
Register type: Read/Write, Read-only
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 8–4. Asynchronous Transmit Retries Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–29	secondLimit	R	The second limit field returns 000b when read, because outbound dual-phase retry is not implemented.
28–16	cycleLimit	R	The cycle limit field returns 0 0000 0000 0000b when read, because outbound dual-phase retry is not implemented.
15–12	RSVD	R	Reserved. Bits 15–12 return 0h when read.
11–8	maxPhysRespRetries	RW	This field tells the physical response unit how many times to attempt to retry the transmit operation for the response packet when a busy acknowledge or ack_data_error is received from the target node. The default value for this field is 0h.
7–4	maxATRespRetries	RW	This field tells the asynchronous transmit response unit how many times to attempt to retry the transmit operation for the response packet when a busy acknowledge or ack_data_error is received from the target node. The default value for this field is 0h.
3–0	maxATReqRetries	RW	This field tells the asynchronous transmit DMA request unit how many times to attempt to retry the transmit operation for the response packet when a busy acknowledge or ack_data_error is received from the target node. The default value for this field is 0h.

8.4 CSR Data Register

The CSR data register accesses the bus management CSR registers from the host through compare-swap operations. This register contains the data to be stored in a CSR if the compare is successful.

OHCI register offset: 0Ch
Register type: Read-only
Default value: XXXX XXXXh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Not Recommended for New Designs

8.5 CSR Compare Register

The CSR compare register accesses the bus management CSR registers from the host through compare-swap operations. This register contains the data to be compared with the existing value of the CSR resource.

OHCI register offset: 10h
Register type: Read-only
Default value: XXXX XXXXh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

8.6 CSR Control Register

The CSR control register accesses the bus management CSR registers from the host through compare-swap operations. This register controls the compare-swap operation and selects the CSR resource. See Table 8–5 for a complete description of the register contents.

OHCI register offset: 14h
Register type: Read/Write, Read/Update, Read-only
Default value: 8000 000Xh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	X	X

Table 8–5. CSR Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	csrDone	RU	Bit 31 is set to 1b by the controller when a compare-swap operation is complete. It is cleared whenever this register is written.
30–2	RSVD	R	Reserved. Bits 30–2 return 0 0000 0000 0000 0000 0000 0000 0000b when read.
1–0	csrSel	RW	This field selects the CSR resource as follows: 00 = BUS_MANAGER_ID 01 = BANDWIDTH_AVAILABLE 10 = CHANNELS_AVAILABLE_HI 11 = CHANNELS_AVAILABLE_LO

Not Recommended for New Designs

8.7 Configuration ROM Header Register

The configuration ROM header register externally maps to the first quadlet of the 1394 configuration ROM, offset FFFF F000 0400h. See Table 8–6 for a complete description of the register contents.

OHCI register offset: 18h
Register type: Read/Write
Default value: 0000 XXXXh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 8–6. Configuration ROM Header Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–24	info_length	RW	IEEE 1394 bus-management field. Must be valid when bit 17 (linkEnable) in the host controller control register at OHCI offset 50h/54h (see Section 8.16) is set to 1b. The default value for this field is 0h.
23–16	crc_length	RW	IEEE 1394 bus-management field. Must be valid when bit 17 (linkEnable) in the host controller control register at OHCI offset 50h/54h (see Section 8.16) is set to 1b. The default value for this field is 0h.
15–0	rom_crc_value	RW	IEEE 1394 bus-management field. Must be valid at any time bit 17 (linkEnable) in the host controller control register at OHCI offset 50h/54h (see Section 8.16) is set to 1b.

8.8 Bus Identification Register

The bus identification register externally maps to the first quadlet in the Bus_Info_Block and contains the constant 3133 3934h, which is the ASCII value of 1394.

OHCI register offset: 1Ch
Register type: Read-only
Default value: 3133 3934h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	1	1	0	0	0	1	0	0	1	1	0	0	1	1
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	1	1	1	0	0	1	0	0	1	1	0	1	0	0

Not Recommended for New Designs

8.9 Bus Options Register

The bus options register externally maps to the second quadlet of the Bus_Info_Block. See Table 8–7 for a complete description of the register contents.

OHCI register offset: 20h
Register type: Read/Write, Read-only
Default value: 0000 A0X2h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	1	0	1	0	0	0	0	0	X	X	0	0	0	0	1	0

Table 8–7. Bus Options Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	irmc	RW	Isochronous resource-manager capable. IEEE 1394 bus-management field. Must be valid when bit 17 (linkEnable) in the host controller control register at OHCI offset 50h/54h (see Section 8.16) is set to 1b. The default value for this bit is 0b.
30	cmc	RW	Cycle master capable. IEEE 1394 bus-management field. Must be valid when bit 17 (linkEnable) in the host controller control register at OHCI offset 50h/54h (see Section 8.16) is set to 1b. The default value for this bit is 0b.
29	isc	RW	Isochronous support capable. IEEE 1394 bus-management field. Must be valid when bit 17 (linkEnable) in the host controller control register at OHCI offset 50h/54h (see Section 8.16) is set to 1b. The default value for this bit is 0b.
28	bmc	RW	Bus manager capable. IEEE 1394 bus-management field. Must be valid when bit 17 (linkEnable) in the host controller control register at OHCI offset 50h/54h (see Section 8.16) is set to 1b. The default value for this bit is 0b.
27	pmc	RW	Power-management capable. IEEE 1394 bus-management field. When bit 27 is set to 1b, this indicates that the node is power-management capable. Must be valid when bit 17 (linkEnable) in the host controller control register at OHCI offset 50h/54h (see Section 8.16) is set to 1b. The default value for this bit is 0b.
26–24	RSVD	R	Reserved. Bits 26–24 return 000b when read.
23–16	cyc_clk_acc	RW	Cycle master clock accuracy, in parts per million. IEEE 1394 bus-management field. Must be valid when bit 17 (linkEnable) in the host controller control register at OHCI offset 50h/54h (see Section 8.16) is set to 1b. The default value for this field is 00h.
15–12 †	max_rec	RW	Maximum request. IEEE 1394 bus-management field. Hardware initializes this field to indicate the maximum number of bytes in a block request packet that is supported by the implementation. This value, max_rec_bytes, must be 512 or greater, and is calculated by 2^(max_rec + 1). Software may change this field; however, this field must be valid at any time bit 17 (linkEnable) in the host controller control register at OHCI offset 50h/54h (see Section 8.16) is set to 1b. A received block write request packet with a length greater than max_rec_bytes may generate an ack_type_error. This field is not affected by a software reset, and defaults to value indicating 2048 bytes on a system (hardware) reset. The default value for this field is Ah.
11–8	RSVD	R	Reserved. Bits 11–8 return 0h when read.
7–6	g	RW	Generation counter. This field is incremented if any portion of the configuration ROM has been incremented since the prior bus reset.
5–3	RSVD	R	Reserved. Bits 5–3 return 000b when read.
2–0	Lnk_spd	R	Link speed. This field returns 010b, indicating that the link speeds of 100M bits/s, 200M bits/s, and 400M bits/s are supported.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Not Recommended for New Designs

8.10 GUID High Register

The GUID high register represents the upper quadlet in a 64-bit global unique ID (GUID) which maps to the third quadlet in the Bus_Info_Block. This register contains node_vendor_ID and chip_ID_hi fields. This register initializes to 0000 0000h on a system (hardware) reset, which is an illegal GUID value. If a serial EEPROM is detected, then the contents of this register are loaded through the serial EEPROM interface. At that point, the contents of this register cannot be changed. If no serial EEPROM is detected, then the contents of this register are loaded by the BIOS. At that point, the contents of this register cannot be changed. This register is reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

OHCI register offset: 24h
Register type: Read-only
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

8.11 GUID Low Register

The GUID low register represents the lower quadlet in a 64-bit global unique ID (GUID) which maps to chip_ID_lo in the Bus_Info_Block. This register initializes to 0000 0000h on a system (hardware) reset and behaves identical to the GUID high register at OHCI offset 24h (see Section 8.10). This register is reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

OHCI register offset: 28h
Register type: Read-only
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

8.12 Configuration ROM Mapping Register

The configuration ROM mapping register contains the start address within system memory that maps to the start address of 1394 configuration ROM for this node. See Table 8–8 for a complete description of the register contents.

OHCI register offset: 34h
Register type: Read/Write
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 8–8. Configuration ROM Mapping Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–10	configROMaddr	RW	If a quadlet read request to 1394 offset FFFF F000 0400h through offset FFFF F000 07FFh is received, then the low-order 10 bits of the offset are added to this register to determine the host memory address of the read request. The default value for this field is all 0s.
9–0	RSVD	R	Reserved. Bits 9–0 return 00 0000 0000b when read.

Not Recommended for New Designs

8.13 Posted Write Address Low Register

The posted write address low register communicates error information if a write request is posted and an error occurs while the posted data packet is being written. See Table 8–9 for a complete description of the register contents.

OHCI register offset: 38h
Register type: Read/Update
Default value: XXXX XXXXh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 8–9. Posted Write Address Low Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–0	offsetLo	RU	The lower 32 bits of the 1394 destination offset of the write request that failed.

8.14 Posted Write Address High Register

The posted write address high register communicates error information if a write request is posted and an error occurs while writing the posted data packet. See Table 8–10 for a complete description of the register contents.

OHCI register offset: 3Ch
Register type: Read/Update
Default value: XXXX XXXXh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 8–10. Posted Write Address High Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–16	sourceID	RU	This field is the 10-bit bus number (bits 31–22) and 6-bit node number (bits 21–16) of the node that issued the write request that failed.
15–0	offsetHi	RU	The upper 16 bits of the 1394 destination offset of the write request that failed.

8.15 Vendor ID Register

The vendor ID register holds the company ID of an organization that specifies any vendor-unique registers. The controller implements Texas Instruments unique behavior with regards to OHCI. Thus, this register is read-only and returns 0108 0028h when read.

OHCI register offset: 40h
Register type: Read-only
Default value: 0108 0028h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0
BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0

Not Recommended for New Designs

8.16 Host Controller Control Register

The host controller control set/clear register pair provides flags for controlling the controller. See Table 8–11 for a complete description of the register contents.

OHCI register offset: 50h set register
54h clear register
Register type: Read/Set/Clear/Update, Read/Set/Clear, Read/Clear, Read-only
Default value: X08X 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	X	0	0	0	0	0	0	1	0	0	0	0	X	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 8–11. Host Controller Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	BIBimage Valid	RSU	When bit 31 is set to 1b, the physical response unit is enabled to respond to block read requests to host configuration ROM and to the mechanism for atomically updating configuration ROM. Software creates a valid image of the bus_info_block in host configuration ROM before setting this bit. When this bit is cleared, the controller returns ack_type_error on block read requests to host configuration ROM. Also, when this bit is cleared and a 1394 bus reset occurs, the configuration ROM mapping register at OHCI offset 34h (see Section 8.12), configuration ROM header register at OHCI offset 18h (see Section 8.7), and bus options register at OHCI offset 20h (see Section 8.9) are not updated. Software can set this bit only when bit 17 (linkEnable) is 0b. Once bit 31 is set to 1b, it can be cleared by a system (hardware) reset, a software reset, or if a fetch error occurs when the controller loads bus_info_block registers from host memory.
30	noByteSwapData	RSC	Bit 30 controls whether physical accesses to locations outside the controller itself, as well as any other DMA data accesses are byte swapped.
29	AckTardyEnable	RSC	Bit 29 controls the acknowledgement of ack_tardy. When bit 29 is set to 1b, ack_tardy may be returned as an acknowledgment to accesses from the 1394 bus to the controller, including accesses to the bus_info_block. The controller returns ack_tardy to all other asynchronous packets addressed to the node. When the controller sends ack_tardy, bit 27 (ack_tardy) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) is set to 1b to indicate the attempted asynchronous access. Software ensures that bit 27 (ack_tardy) in the interrupt event register is 0b. Software also unmasks wake-up interrupt events such as bit 19 (phy) and bit 27 (ack_tardy) in the interrupt event register before placing the controller into the D1 power mode. Software must not set this bit if the node is the 1394 bus manager.
28–24	RSVD	R	Reserved. Bits 28–24 return 00000b when read.
23 †	programPhyEnable	R	Bit 23 informs upper-level software that lower-level software has consistently configured the IEEE 1394a-2000 enhancements in the link and PHY layers. When this bit is 1b, generic software such as the OHCI driver is responsible for configuring IEEE 1394a-2000 enhancements in the PHY layer and bit 22 (aPhyEnhanceEnable). When this bit is 0b, the generic software may not modify the IEEE 1394a-2000 enhancements in the PHY layer and cannot interpret the setting of bit 22 (aPhyEnhanceEnable). This bit is initialized from serial EEPROM. This bit defaults to 1b.
22	aPhyEnhanceEnable	RSC	When bits 23 (programPhyEnable) and 17 (linkEnable) are 11b, the OHCI driver can set bit 22 to 1b to use all IEEE 1394a-2000 enhancements. When bit 23 (programPhyEnable) is cleared to 0b, the software does not change PHY enhancements or this bit.
21–20	RSVD	R	Reserved. Bits 21 and 20 return 00b when read.

† This bit is reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Not Recommended for New Designs

Table 8–11. Host Controller Control Register Description (Continued)

BIT	FIELD NAME	TYPE	DESCRIPTION
19	LPS	RSC	Bit 19 controls the link power status. Software must set this bit to 1b to permit the link-PHY communication. A 0b prevents link-PHY communication. The OHCI-link is divided into two clock domains (PCLK and PHY_SCLK). If software tries to access any register in the PHY_SCLK domain while the PHY_SCLK is disabled, then a target abort is issued by the link. This problem can be avoided by setting bit 4 (DIS_TGT_ABT) to 1b in the PCI miscellaneous configuration register at offset F0h in the PCI configuration space (see Section 7.22). This allows the link to respond to these types of request by returning all Fs (hex). OHCI registers at offsets DCh–F0h and 100h–11Ch are in the PHY_SCLK domain. After setting LPS, software must wait approximately 10 ms before attempting to access any of the OHCI registers. This gives the PHY_SCLK time to stabilize.
18	postedWriteEnable	RSC	Bit 18 enables (1) or disables (0) posted writes. Software changes this bit only when bit 17 (linkEnable) is 0b.
17	linkEnable	RSC	Bit 17 is cleared to 0b by either a system (hardware) or software reset. Software must set this bit to 1b when the system is ready to begin operation and then force a bus reset. This bit is necessary to keep other nodes from sending transactions before the local system is ready. When this bit is cleared, the controller is logically and immediately disconnected from the 1394 bus, no packets are received or processed, nor are packets transmitted.
16	SoftReset	RSCU	When bit 16 is set to 1b, all states are reset, all FIFOs are flushed, and all OHCI registers are set to their system (hardware) reset values, unless otherwise specified. PCI registers are not affected by this bit. This bit remains set to 1b while the software reset is in progress and reverts back to 0b when the reset has completed.
15–0	RSVD	R	Reserved. Bits 15–0 return 0000h when read.

8.17 Self-ID Buffer Pointer Register

The self-ID buffer pointer register points to the 2K-byte aligned base address of the buffer in host memory where the self-ID packets are stored during bus initialization. Bits 31–11 are read/write accessible. Bits 10–0 are reserved, and return 000 0000 0000b when read.

OHCI register offset: 64h
Register type: Read/Write, Read-only
Default value: XXXX XX00h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	X	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0

Not Recommended for New Designs

8.18 Self-ID Count Register

The self-ID count register keeps a count of the number of times the bus self-ID process has occurred, flags self-ID packet errors, and keeps a count of the self-ID data in the self-ID buffer. See Table 8–12 for a complete description of the register contents.

OHCI register offset: 68h
Register type: Read/Update, Read-only
Default value: X0XX 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	X	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 8–12. Self-ID Count Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	selfIDError	RU	When bit 31 is set to 1b, an error was detected during the most recent self-ID packet reception. The contents of the self-ID buffer are undefined. This bit is cleared after a self-ID reception in which no errors are detected. Note that an error can be a hardware error or a host bus write error.
30–24	RSVD	R	Reserved. Bits 30–24 return 000 0000b when read.
23–16	selfIDGeneration	RU	The value in this field increments each time a bus reset is detected. This field rolls over to 0 after reaching 255.
15–11	RSVD	R	Reserved. Bits 15–11 return 00000b when read.
10–2	selfIDSize	RU	This field indicates the number of quadlets that have been written into the self-ID buffer for the current bits 23–16 (selfIDGeneration field). This includes the header quadlet and the self-ID data. This field is cleared to 0 0000 0000b when the self-ID reception begins.
1–0	RSVD	R	Reserved. Bits 1 and 0 return 00b when read.

Not Recommended for New Designs

8.19 Isochronous Receive Channel Mask High Register

The isochronous receive channel mask high set/clear register enables packet receives from the upper 32 isochronous data channels. A read from either the set or clear register returns the content of the isochronous receive channel mask high register. See Table 8–13 for a complete description of the register contents.

OHCI register offset: 70h set register
74h clear register
Register type: Read/Set/Clear
Default value: XXXX XXXXh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 8–13. Isochronous Receive Channel Mask High Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	isoChannel63	RSC	When bit 31 is set to 1b, the controller is enabled to receive from isochronous channel number 63.
30	isoChannel62	RSC	When bit 30 is set to 1b, the controller is enabled to receive from isochronous channel number 62.
29	isoChannel61	RSC	When bit 29 is set to 1b, the controller is enabled to receive from isochronous channel number 61.
28	isoChannel60	RSC	When bit 28 is set to 1b, the controller is enabled to receive from isochronous channel number 60.
27	isoChannel59	RSC	When bit 27 is set to 1b, the controller is enabled to receive from isochronous channel number 59.
26	isoChannel58	RSC	When bit 26 is set to 1b, the controller is enabled to receive from isochronous channel number 58.
25	isoChannel57	RSC	When bit 25 is set to 1b, the controller is enabled to receive from isochronous channel number 57.
24	isoChannel56	RSC	When bit 24 is set to 1b, the controller is enabled to receive from isochronous channel number 56.
23	isoChannel55	RSC	When bit 23 is set to 1b, the controller is enabled to receive from isochronous channel number 55.
22	isoChannel54	RSC	When bit 22 is set to 1b, the controller is enabled to receive from isochronous channel number 54.
21	isoChannel53	RSC	When bit 21 is set to 1b, the controller is enabled to receive from isochronous channel number 53.
20	isoChannel52	RSC	When bit 20 is set to 1b, the controller is enabled to receive from isochronous channel number 52.
19	isoChannel51	RSC	When bit 19 is set to 1b, the controller is enabled to receive from isochronous channel number 51.
18	isoChannel50	RSC	When bit 18 is set to 1b, the controller is enabled to receive from isochronous channel number 50.
17	isoChannel49	RSC	When bit 17 is set to 1b, the controller is enabled to receive from isochronous channel number 49.
16	isoChannel48	RSC	When bit 16 is set to 1b, the controller is enabled to receive from isochronous channel number 48.
15	isoChannel47	RSC	When bit 15 is set to 1b, the controller is enabled to receive from isochronous channel number 47.
14	isoChannel46	RSC	When bit 14 is set to 1b, the controller is enabled to receive from isochronous channel number 46.
13	isoChannel45	RSC	When bit 13 is set to 1b, the controller is enabled to receive from isochronous channel number 45.
12	isoChannel44	RSC	When bit 12 is set to 1b, the controller is enabled to receive from isochronous channel number 44.
11	isoChannel43	RSC	When bit 11 is set to 1b, the controller is enabled to receive from isochronous channel number 43.
10	isoChannel42	RSC	When bit 10 is set to 1b, the controller is enabled to receive from isochronous channel number 42.
9	isoChannel41	RSC	When bit 9 is set to 1b, the controller is enabled to receive from isochronous channel number 41.
8	isoChannel40	RSC	When bit 8 is set to 1b, the controller is enabled to receive from isochronous channel number 40.
7	isoChannel39	RSC	When bit 7 is set to 1b, the controller is enabled to receive from isochronous channel number 39.
6	isoChannel38	RSC	When bit 6 is set to 1b, the controller is enabled to receive from isochronous channel number 38.
5	isoChannel37	RSC	When bit 5 is set to 1b, the controller is enabled to receive from isochronous channel number 37.
4	isoChannel36	RSC	When bit 4 is set to 1b, the controller is enabled to receive from isochronous channel number 36.
3	isoChannel35	RSC	When bit 3 is set to 1b, the controller is enabled to receive from isochronous channel number 35.
2	isoChannel34	RSC	When bit 2 is set to 1b, the controller is enabled to receive from isochronous channel number 34.
1	isoChannel33	RSC	When bit 1 is set to 1b, the controller is enabled to receive from isochronous channel number 33.
0	isoChannel32	RSC	When bit 0 is set to 1b, the controller is enabled to receive from isochronous channel number 32.

Not Recommended for New Designs

8.20 Isochronous Receive Channel Mask Low Register

The isochronous receive channel mask low set/clear register enables packet receives from the lower 32 isochronous data channels. See Table 8−14 for a complete description of the register contents.

OHCI register offset: 78h set register
7Ch clear register
Register type: Read/Set/Clear
Default value: XXXX XXXXh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 8−14. Isochronous Receive Channel Mask Low Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	isoChannel31	RSC	When bit 31 is set to 1b, the controller is enabled to receive from isochronous channel number 31.
30	isoChannel30	RSC	When bit 30 is set to 1b, the controller is enabled to receive from isochronous channel number 30.
29−2	isoChannelN	RSC	Bits 29 through 2 (isoChannelN, where n = 29, 28, 27, …, 2) follow the same pattern as bits 31 and 30.
1	isoChannel1	RSC	When bit 1 is set to 1b, the controller is enabled to receive from isochronous channel number 1.
0	isoChannel0	RSC	When bit 0 is set to 1b, the controller is enabled to receive from isochronous channel number 0.

Not Recommended for New Designs

8.21 Interrupt Event Register

The interrupt event set/clear register reflects the state of the various interrupt sources. The interrupt bits are set to 1b by an asserting edge of the corresponding interrupt signal or by writing a 1b in the corresponding bit in the set register. The only mechanism to clear a bit in this register is to write a 1b to the corresponding bit in the clear register.

This register is fully compliant with the *1394 Open Host Controller Interface Specification*, and the controller adds a vendor-specific interrupt function to bit 30. When the interrupt event register is read, the return value is the bit-wise AND function of the interrupt event and interrupt mask registers. See Table 8–15 for a complete description of the register contents.

OHCI register offset: 80h set register
84h clear register [returns the content of the interrupt event register bit-wise ANDed with the interrupt mask register when read]
Register type: Read/Set/Clear/Update, Read/Set/Clear, Read/Update, Read-only
Default value: XXXX 0XXXh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	X	0	0	0	X	X	X	X	X	X	X	X	0	X	X
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X

Table 8–15. Interrupt Event Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–30	RSVD	R	Reserved. Bits 31 and 30 return 00b when read.
29	SoftInterrupt	RSC	Bit 29 is used by software to generate an interrupt for its own use.
28	RSVD	R	Reserved. Bit 28 returns 0b when read.
27	ack_tardy	RSCU	Bit 27 is set to 1b when bit 29 (AckTardyEnable) in the host controller control register at OHCI offset 50h/54h (see Section 8.16) is set to 1b and any of the following conditions occur: a. Data is present in a receive FIFO that is to be delivered to the host. b. The physical response unit is busy processing requests or sending responses. c. The controller sent an ack_tardy acknowledgment.
26	phyRegRcvd	RSCU	The controller has received a PHY register data byte which can be read from bits 23–16 in the PHY layer control register at OHCI offset ECh (see Section 8.33).
25	cycleTooLong	RSCU	If bit 21 (cycleMaster) in the link control register at OHCI offset E0h/E4h (see Section 8.31) is set to 1b, then this indicates that over 125 µs has elapsed between the start of sending a cycle start packet and the end of a subaction gap. Bit 21 (cycleMaster) in the link control register is cleared by this event.
24	unrecoverableError	RSCU	This event occurs when the controller encounters any error that forces it to stop operations on any or all of its subunits, for example, when a DMA context sets its dead bit to 1b. While bit 24 is set to 1b, all normal interrupts for the context(s) that caused this interrupt are blocked from being set to 1b.
23	cycleInconsistent	RSCU	A cycle start was received that had values for the cycleSeconds and cycleCount fields that are different from the values in bits 31–25 (cycleSeconds field) and bits 24–12 (cycleCount field) in the isochronous cycle timer register at OHCI offset F0h (see Section 8.34).
22	cycleLost	RSCU	A lost cycle is indicated when no cycle_start packet is sent or received between two successive cycleSynch events. A lost cycle can be predicted when a cycle_start packet does not immediately follow the first subaction gap after the cycleSynch event or if an arbitration reset gap is detected after a cycleSynch event without an intervening cycle start. Bit 22 may be set to 1b either when a lost cycle occurs or when logic predicts that one will occur.
21	cycle64Seconds	RSCU	Indicates that the seventh bit of the cycle second counter has changed.
20	cycleSynch	RSCU	Indicates that a new isochronous cycle has started. Bit 20 is set to 1b when the low-order bit of the cycle count toggles.
19	phy	RSCU	Indicates that the PHY layer requests an interrupt through a status transfer.
18	regAccessFail	RSCU	Indicates that a register access has failed due to a missing SCLK clock signal from the PHY layer. When a register access fails, bit 18 is set to 1b before the next register access.

Not Recommended for New Designs

Table 8–15. Interrupt Event Register Description (Continued)

BIT	FIELD NAME	TYPE	DESCRIPTION
17	busReset	RSCU	Indicates that the PHY layer has entered bus reset mode.
16	selfIDcomplete	RSCU	A self-ID packet stream has been received. It is generated at the end of the bus initialization process. Bit 16 is turned off simultaneously when bit 17 (busReset) is turned on.
15	selfIDcomplete2	RSCU	Secondary indication of the end of a self-ID packet stream. Bit 15 is set to 1b by the controller when it sets bit 16 (selfIDcomplete), and retains the state, independent of bit 17 (busReset).
14–10	RSVD	R	Reserved. Bits 14–10 return 00000b when read.
9	lockRespErr	RSCU	Indicates that the controller sent a lock response for a lock request to a serial bus register, but did not receive an ack_complete.
8	postedWriteErr	RSCU	Indicates that a host bus error occurred while the controller was trying to write a 1394 write request, which had already been given an ack_complete, into system memory.
7	isochRx	RU	Isochronous receive DMA interrupt. Indicates that one or more isochronous receive contexts have generated an interrupt. This is not a latched event; it is the logical OR of all bits in the isochronous receive interrupt event register at OHCI offset A0h/A4h (see Section 8.25) and isochronous receive interrupt mask register at OHCI offset A8h/ACh (see Section 8.26). The isochronous receive interrupt event register indicates which contexts have been interrupted.
6	isochTx	RU	Isochronous transmit DMA interrupt. Indicates that one or more isochronous transmit contexts have generated an interrupt. This is not a latched event; it is the logical OR of all bits in the isochronous transmit interrupt event register at OHCI offset 90h/94h (see Section 8.23) and isochronous transmit interrupt mask register at OHCI offset 98h/9Ch (see Section 8.24). The isochronous transmit interrupt event register indicates which contexts have been interrupted.
5	RSPkt	RSCU	Indicates that a packet was sent to an asynchronous receive response context buffer and the descriptor xferStatus and resCount fields have been updated.
4	RQPkt	RSCU	Indicates that a packet was sent to an asynchronous receive request context buffer and the descriptor xferStatus and resCount fields have been updated.
3	ARRS	RSCU	Asynchronous receive response DMA interrupt. Bit 3 is conditionally set to 1b upon completion of an ARRS DMA context command descriptor.
2	ARRQ	RSCU	Asynchronous receive request DMA interrupt. Bit 2 is conditionally set to 1b upon completion of an ARRQ DMA context command descriptor.
1	respTxComplete	RSCU	Asynchronous response transmit DMA interrupt. Bit 1 is conditionally set to 1b upon completion of an ATRS DMA command.
0	reqTxComplete	RSCU	Asynchronous request transmit DMA interrupt. Bit 0 is conditionally set to 1b upon completion of an ATRQ DMA command.

Not Recommended for New Designs

8.22 Interrupt Mask Register

The interrupt mask set/clear register enables the various interrupt sources. Reads from either the set register or the clear register always return the contents of the interrupt mask register. In all cases except masterIntEnable (bit 31) and vendorSpecific (bit 30), the enables for each interrupt event align with the interrupt event register bits detailed in Table 8–15.

This register is fully compliant with the *1394 Open Host Controller Interface Specification* and the controller adds an interrupt function to bit 30. See Table 8–16 for a complete description of bits 31 and 30.

OHCI register offset: 88h set register
8Ch clear register
Register type: Read/Set/Clear/Update, Read/Set/Clear, Read/Update, Read-only
Default value: XXXX 0XXXh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	X	X	0	0	0	X	X	X	X	X	X	X	X	0	X	X
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X

Table 8–16. Interrupt Mask Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	masterIntEnable	RSCU	Master interrupt enable. If bit 31 is set to 1b, then external interrupts are generated in accordance with the interrupt mask register. If this bit is cleared, then external interrupts are not generated regardless of the interrupt mask register settings.
30	VendorSpecific	RSC	When this bit and bit 30 (vendorSpecific) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this vendor-specific interrupt mask enables interrupt generation.
29	SoftInterrupt	RSC	When this bit and bit 29 (SoftInterrupt) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this soft-interrupt mask enables interrupt generation.
28	RSVD	R	Reserved. Bit 28 returns 0b when read.
27	ack_tardy	RSC	When this bit and bit 27 (ack_tardy) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this acknowledge-tardy interrupt mask enables interrupt generation.
26	phyRegRcvd	RSC	When this bit and bit 26 (phyRegRcvd) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this PHY-register interrupt mask enables interrupt generation.
25	cycleTooLong	RSC	When this bit and bit 25 (cycleTooLong) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this cycle-too-long interrupt mask enables interrupt generation.
24	unrecoverableError	RSC	When this bit and bit 24 (unrecoverableError) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this unrecoverable-error interrupt mask enables interrupt generation.
23	cycleInconsistent	RSC	When this bit and bit 23 (cycleInconsistent) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this inconsistent-cycle interrupt mask enables interrupt generation.
22	cycleLost	RSC	When this bit and bit 22 (cycleLost) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this lost-cycle interrupt mask enables interrupt generation.
21	cycle64Seconds	RSC	When this bit and bit 21 (cycle64Seconds) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this 64-second-cycle interrupt mask enables interrupt generation.
20	cycleSynch	RSC	When this bit and bit 20 (cycleSynch) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this isochronous-cycle interrupt mask enables interrupt generation.
19	phy	RSC	When this bit and bit 19 (phy) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this PHY-status-transfer interrupt mask enables interrupt generation.
18	regAccessFail	RSC	When this bit and bit 18 (regAccessFail) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this register-access-failed interrupt mask enables interrupt generation.
17	busReset	RSC	When this bit and bit 17 (busReset) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this bus-reset interrupt mask enables interrupt generation.
16	selfIDcomplete	RSC	When this bit and bit 16 (selfIDcomplete) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this self-ID-complete interrupt mask enables interrupt generation.

Not Recommended for New Designs

Table 8–16. Interrupt Mask Register Description (Continued)

BIT	FIELD NAME	TYPE	DESCRIPTION
15	selfIDcomplete2	RSC	When this bit and bit 15 (selfIDcomplete2) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this second-self-ID-complete interrupt mask enables interrupt generation.
14–10	RSVD	R	Reserved. Bits 14–10 return 00000b when read.
9	lockRespErr	RSC	When this bit and bit 9 (lockRespErr) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this lock-response-error interrupt mask enables interrupt generation.
8	postedWriteErr	RSC	When this bit and bit 8 (postedWriteErr) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this posted-write-error interrupt mask enables interrupt generation.
7	isochRx	RSC	When this bit and bit 7 (isochRx) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this isochronous-receive-DMA interrupt mask enables interrupt generation.
6	isochTx	RSC	When this bit and bit 6 (isochTx) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this isochronous-transmit-DMA interrupt mask enables interrupt generation.
5	RSPkt	RSC	When this bit and bit 5 (RSPkt) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this receive-response-packet interrupt mask enables interrupt generation.
4	RQPkt	RSC	When this bit and bit 4 (RQPkt) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this receive-request-packet interrupt mask enables interrupt generation.
3	ARRS	RSC	When this bit and bit 3 (ARRS) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this asynchronous-receive-response-DMA interrupt mask enables interrupt generation.
2	ARRQ	RSC	When this bit and bit 2 (ARRQ) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this asynchronous-receive-request-DMA interrupt mask enables interrupt generation.
1	respTxComplete	RSC	When this bit and bit 1 (respTxComplete) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this response-transmit-complete interrupt mask enables interrupt generation.
0	reqTxComplete	RSC	When this bit and bit 0 (reqTxComplete) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) are set to 11b, this request-transmit-complete interrupt mask enables interrupt generation.

Not Recommended for New Designs

8.23 Isochronous Transmit Interrupt Event Register

The isochronous transmit interrupt event set/clear register reflects the interrupt state of the isochronous transmit contexts. An interrupt is generated on behalf of an isochronous transmit context if an OUTPUT_LAST* command completes and its interrupt bits are set to 1. Upon determining that the isochTx (bit 6) interrupt has occurred in the interrupt event register at OHCI offset 80h/84h (see Section 8.21), software can check this register to determine which context(s) caused the interrupt. The interrupt bits are set to 1 by an asserting edge of the corresponding interrupt signal, or by writing a 1b in the corresponding bit in the set register. The only mechanism to clear a bit in this register is to write a 1b to the corresponding bit in the clear register. See Table 8–17 for a complete description of the register contents.

OHCI register offset: 90h set register
94h clear register [returns the contents of the isochronous transmit interrupt event register bit-wise ANDed with the isochronous transmit interrupt mask register when read]
Register type: Read/Set/Clear, Read-only
Default value: 0000 00XXh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X

Table 8–17. Isochronous Transmit Interrupt Event Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–8	RSVD	R	Reserved. Bits 31–8 return 0000h when read.
7	isoXmit7	RSC	Isochronous transmit channel 7 caused the interrupt event register bit 6 (isochTx) interrupt.
6	isoXmit6	RSC	Isochronous transmit channel 6 caused the interrupt event register bit 6 (isochTx) interrupt.
5	isoXmit5	RSC	Isochronous transmit channel 5 caused the interrupt event register bit 6 (isochTx) interrupt.
4	isoXmit4	RSC	Isochronous transmit channel 4 caused the interrupt event register bit 6 (isochTx) interrupt.
3	isoXmit3	RSC	Isochronous transmit channel 3 caused the interrupt event register bit 6 (isochTx) interrupt.
2	isoXmit2	RSC	Isochronous transmit channel 2 caused the interrupt event register bit 6 (isochTx) interrupt.
1	isoXmit1	RSC	Isochronous transmit channel 1 caused the interrupt event register bit 6 (isochTx) interrupt.
0	isoXmit0	RSC	Isochronous transmit channel 0 caused the interrupt event register bit 6 (isochTx) interrupt.

8.24 Isochronous Transmit Interrupt Mask Register

The isochronous transmit interrupt mask set/clear register enables the isochTx interrupt source on a per-channel basis. Reads from either the set register or the clear register always return the contents of the isochronous transmit interrupt mask register. In all cases the enables for each interrupt event align with the isochronous transmit interrupt event register bits detailed in Table 8–17.

OHCI register offset: 98h set register
9Ch clear register
Register type: Read/Set/Clear, Read-only
Default value: 0000 00XXh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X

Not Recommended for New Designs

8.25 Isochronous Receive Interrupt Event Register

The isochronous receive interrupt event set/clear register reflects the interrupt state of the isochronous receive contexts. An interrupt is generated on behalf of an isochronous receive context if an INPUT_* command completes and its interrupt bits are set to 1. Upon determining that the isochRx (bit 7) interrupt in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) has occurred, software can check this register to determine which context(s) caused the interrupt. The interrupt bits are set to 1 by an asserting edge of the corresponding interrupt signal or by writing a 1b in the corresponding bit in the set register. The only mechanism to clear a bit in this register is to write a 1b to the corresponding bit in the clear register. See Table 8–18 for a complete description of the register contents.

OHCI register offset: A0h set register
A4h clear register [returns the contents of isochronous receive interrupt event register bit-wise ANDed with the isochronous receive mask register when read]
Register type: Read/Set/Clear, Read-only
Default value: 0000 000Xh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	X	X	X	X

Table 8–18. Isochronous Receive Interrupt Event Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–4	RSVD	R	Reserved. Bits 31–4 return 000 0000h when read.
3	isoRecv3	RSC	Isochronous receive channel 3 caused the interrupt event register bit 7 (isochRx) interrupt.
2	isoRecv2	RSC	Isochronous receive channel 2 caused the interrupt event register bit 7 (isochRx) interrupt.
1	isoRecv1	RSC	Isochronous receive channel 1 caused the interrupt event register bit 7 (isochRx) interrupt.
0	isoRecv0	RSC	Isochronous receive channel 0 caused the interrupt event register bit 7 (isochRx) interrupt.

8.26 Isochronous Receive Interrupt Mask Register

The isochronous receive interrupt mask set/clear register enables the isochRx interrupt source on a per-channel basis. Reads from either the set register or the clear register always return the contents of the isochronous receive interrupt mask register. In all cases the enables for each interrupt event align with the isochronous receive interrupt event register bits detailed in Table 8–18.

OHCI register offset: A8h set register
ACh clear register
Register type: Read/Set/Clear, Read-only
Default value: 0000 000Xh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	X	X	X	X

Not Recommended for New Designs

8.27 Initial Bandwidth Available Register

The initial bandwidth available register value is loaded into the corresponding bus management CSR register on a system (hardware) or software reset. See Table 8–19 for a complete description of the register contents.

OHCI register offset: B0h
Register type: Read-only, Read/Write
Default value: 0000 1333h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	1	0	0	1	1	0	0	1	1	0	0	1	1

Table 8–19. Initial Bandwidth Available Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–13	RSVD	R	Reserved. Bits 31–13 return 000 0000 0000 0000 0000b when read.
12–0	InitBWAvailable	RW	This field is reset to 1333h on a system (hardware) or software reset, and is not affected by a 1394 bus reset. The value of this field is loaded into the BANDWIDTH_AVAILABLE CSR register upon a $\overline{\text{GRST}}$, $\overline{\text{PERST}}$, $\overline{\text{PRST}}$, or a 1394 bus reset.

8.28 Initial Channels Available High Register

The initial channels available high register value is loaded into the corresponding bus management CSR register on a system (hardware) or software reset. See Table 8–20 for a complete description of the register contents.

OHCI register offset: B4h
Register type: Read/Write
Default value: FFFF FFFFh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 8–20. Initial Channels Available High Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–0	InitChanAvailHi	RW	This field is reset to FFFF_FFFFh on a system (hardware) or software reset, and is not affected by a 1394 bus reset. The value of this field is loaded into the CHANNELS_AVAILABLE_HI CSR register upon a $\overline{\text{GRST}}$, $\overline{\text{PERST}}$, $\overline{\text{PRST}}$, or a 1394 bus reset.

Not Recommended for New Designs

8.29 Initial Channels Available Low Register

The initial channels available low register value is loaded into the corresponding bus management CSR register on a system (hardware) or software reset. See Table 8–21 for a complete description of the register contents.

OHCI register offset: B8h
Register type: Read/Write
Default value: FFFF FFFFh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 8–21. Initial Channels Available Low Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–0	InitChanAvailLo	RW	This field is reset to FFFF_FFFFh on a system (hardware) or software reset, and is not affected by a 1394 bus reset. The value of this field is loaded into the CHANNELS_AVAILABLE_LO CSR register upon a $\overline{\text{GRST}}$, $\overline{\text{PRST}}$, $\overline{\text{PRST}}$, or a 1394 bus reset.

8.30 Fairness Control Register

The fairness control register provides a mechanism by which software can direct the host controller to transmit multiple asynchronous requests during a fairness interval. See Table 8–22 for a complete description of the register contents.

OHCI register offset: DCh
Register type: Read-only
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 8–22. Fairness Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–8	RSVD	R	Reserved. Bits 31–8 return 00 0000h when read.
7–0	pri_req	RW	This field specifies the maximum number of priority arbitration requests for asynchronous request packets that the link is permitted to make of the PHY layer during a fairness interval. The default value for this field is 00h.

Not Recommended for New Designs

8.31 Link Control Register

The link control set/clear register provides the control flags that enable and configure the link core protocol portions of the controller. It contains controls for the receiver and cycle timer. See Table 8–23 for a complete description of the register contents.

OHCI register offset: E0h set register
E4h clear register
Register type: Read/Set/Clear/Update, Read/Set/Clear, Read-only
Default value: 00X0 0X00h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	X	X	X	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	X	X	0	0	0	0	0	0	0	0	0

Table 8–23. Link Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–23	RSVD	R	Reserved. Bits 31–23 return 0 0000 0000b when read.
22	cycleSource	RSC	When bit 22 is set to 1b, the cycle timer uses an external source (CYCLEIN) to determine when to roll over the cycle timer. When this bit is cleared, the cycle timer rolls over when the timer reaches 3072 cycles of the 24.576-MHz clock (125 µs).
21	cycleMaster	RSCU	When bit 21 is set to 1b, the controller is root and it generates a cycle start packet every time the cycle timer rolls over, based on the setting of bit 22 (cycleSource). When bit 21 is cleared, the OHCI-Lynx™ accepts received cycle start packets to maintain synchronization with the node which is sending them. Bit 21 is automatically cleared when bit 25 (cycleTooLong) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) is set to 1b. Bit 21 cannot be set to 1b until bit 25 (cycleTooLong) is cleared.
20	CycleTimerEnable	RSC	When bit 20 is set to 1b, the cycle timer offset counts cycles of the 24.576-MHz clock and rolls over at the appropriate time, based on the settings of the above bits. When this bit is cleared, the cycle timer offset does not count.
19–11	RSVD	R	Reserved. Bits 19–11 return 0 0000 0000b when read.
10	RcvPhyPkt	RSC	When bit 10 is set to 1b, the receiver accepts incoming PHY packets into the AR request context if the AR request context is enabled. This bit does not control receipt of self-identification packets.
9	RcvSelfID	RSC	When bit 9 is set to 1b, the receiver accepts incoming self-identification packets. Before setting this bit to 1b, software must ensure that the self-ID buffer pointer register contains a valid address.
8–7	RSVD	R	Reserved. Bits 8 and 7 return 00b when read.
6 †	tag1SyncFilterLock	RS	When bit 6 is set to 1b, bit 6 (tag1SyncFilter) in the isochronous receive context match register (see Section 8.46) is set to 1b for all isochronous receive contexts. When bit 6 is cleared, bit 6 (tag1SyncFilter) in the isochronous receive context match register has read/write access.
5–0	RSVD	R	Reserved. Bits 5–0 return 00 0000b when read.

† This bit is reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Not Recommended for New Designs

8.32 Node Identification Register

The node identification register contains the address of the node on which the OHCI-Lynx™ chip resides, and indicates the valid node number status. The 16-bit combination of the busNumber field (bits 15–6) and the NodeNumber field (bits 5–0) is referred to as the node ID. See Table 8–24 for a complete description of the register contents.

OHCI register offset: E8h
Register type: Read/Write/Update, Read/Update, Read-only
Default value: 0000 FFXXh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	1	1	1	1	1	1	1	1	1	1	X	X	X	X	X	X

Table 8–24. Node Identification Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	iDValid	RU	Bit 31 indicates whether or not the controller has a valid node number. It is cleared when a 1394 bus reset is detected and set to 1b when the controller receives a new node number from its PHY layer.
30	root	RU	Bit 30 is set to 1b during the bus reset process if the attached PHY layer is root.
29–28	RSVD	R	Reserved. Bits 29 and 28 return 00b when read.
27	CPS	RU	Bit 27 is set to 1b if the PHY layer is reporting that cable power status is OK.
26–16	RSVD	R	Reserved. Bits 26–16 return 000 0000 0000b when read.
15–6	busNumber	RWU	This field identifies the specific 1394 bus the controller belongs to when multiple 1394-compatible buses are connected via a bridge. The default value for this field is all 1s.
5–0	NodeNumber	RU	This field is the physical node number established by the PHY layer during self-identification. It is automatically set to the value received from the PHY layer after the self-identification phase. If the PHY layer sets the nodeNumber to 63, then software must not set bit 15 (run) in the asynchronous context control register (see Section 8.40) for either of the AT DMA contexts.

Not Recommended for New Designs

8.33 PHY Layer Control Register

The PHY layer control register reads from or writes to a PHY register. See Table 8–25 for a complete description of the register contents.

OHCI register offset: ECh
Register type: Read/Write/Update, Read/Write, Read/Update, Read-only
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 8–25. PHY Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	rdDone	RU	Bit 31 is cleared to 0b by the controller when either bit 15 (rdReg) or bit 14 (wrReg) is set to 1b. This bit is set to 1b when a register transfer is received from the PHY layer.
30–28	RSVD	R	Reserved. Bits 30–28 return 000b when read.
27–24	rdAddr	RU	This field is the address of the register most recently received from the PHY layer.
23–16	rdData	RU	This field is the contents of a PHY register that has been read.
15	rdReg	RWU	Bit 15 is set to 1b by software to initiate a read request to a PHY register, and is cleared by hardware when the request has been sent. Bits 14 (wrReg) and 15 (rdReg) must not both be set to 1b simultaneously.
14	wrReg	RWU	Bit 14 is set to 1b by software to initiate a write request to a PHY register, and is cleared by hardware when the request has been sent. Bits 14 (wrReg) and 15 (rdReg) must not both be set to 1b simultaneously.
13–12	RSVD	R	Reserved. Bits 13 and 12 return 00b when read.
11–8	regAddr	RW	This field is the address of the PHY register to be written or read. The default value for this field is 0h.
7–0	wrData	RW	This field is the data to be written to a PHY register and is ignored for reads. The default value for this field is 00h.

8.34 Isochronous Cycle Timer Register

The isochronous cycle timer register indicates the current cycle number and offset. When the controller is cycle master, this register is transmitted with the cycle start message. When the controller is not cycle master, this register is loaded with the data field in an incoming cycle start. In the event that the cycle start message is not received, the fields can continue incrementing on their own (if programmed) to maintain a local time reference. See Table 8–26 for a complete description of the register contents.

OHCI register offset: F0h
Register type: Read/Write/Update
Default value: XXXX XXXXh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
BIT NUMBER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 8–26. Isochronous Cycle Timer Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–25	cycleSeconds	RWU	This field counts seconds [rollovers from bits 24–12 (cycleCount field)] modulo 128.
24–12	cycleCount	RWU	This field counts cycles [rollovers from bits 11–0 (cycleOffset field)] modulo 8000.
11–0	cycleOffset	RWU	This field counts 24.576-MHz clocks modulo 3072, that is, 125 µs. If an external 8-kHz clock configuration is being used, then this field must be cleared to 000h at each tick of the external clock.

Not Recommended for New Designs

8.35 Asynchronous Request Filter High Register

The asynchronous request filter high set/clear register enables asynchronous receive requests on a per-node basis, and handles the upper node IDs. When a packet is destined for either the physical request context or the ARRQ context, the source node ID is examined. If the bit corresponding to the node ID is not set to 1b in this register, then the packet is not acknowledged and the request is not queued. The node ID comparison is done if the source node is on the same bus as the controller. Nonlocal bus-sourced packets are not acknowledged unless bit 31 in this register is set to 1b. See Table 8–27 for a complete description of the register contents.

OHCI register offset: 100h set register
104h clear register
Register type: Read/Set/Clear
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 8–27. Asynchronous Request Filter High Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	asynReqAllBuses	RSC	If bit 31 is set to 1b, then all asynchronous requests received by the controller from nonlocal bus nodes are accepted.
30	asynReqResource62	RSC	If bit 30 is set to 1b for local bus node number 62, then asynchronous requests received by the controller from that node are accepted.
29	asynReqResource61	RSC	If bit 29 is set to 1b for local bus node number 61, then asynchronous requests received by the controller from that node are accepted.
28	asynReqResource60	RSC	If bit 28 is set to 1b for local bus node number 60, then asynchronous requests received by the controller from that node are accepted.
27	asynReqResource59	RSC	If bit 27 is set to 1b for local bus node number 59, then asynchronous requests received by the controller from that node are accepted.
26	asynReqResource58	RSC	If bit 26 is set to 1b for local bus node number 58, then asynchronous requests received by the controller from that node are accepted.
25	asynReqResource57	RSC	If bit 25 is set to 1b for local bus node number 57, then asynchronous requests received by the controller from that node are accepted.
24	asynReqResource56	RSC	If bit 24 is set to 1b for local bus node number 56, then asynchronous requests received by the controller from that node are accepted.
23	asynReqResource55	RSC	If bit 23 is set to 1b for local bus node number 55, then asynchronous requests received by the controller from that node are accepted.
22	asynReqResource54	RSC	If bit 22 is set to 1b for local bus node number 54, then asynchronous requests received by the controller from that node are accepted.
21	asynReqResource53	RSC	If bit 21 is set to 1b for local bus node number 53, then asynchronous requests received by the controller from that node are accepted.
20	asynReqResource52	RSC	If bit 20 is set to 1b for local bus node number 52, then asynchronous requests received by the controller from that node are accepted.
19	asynReqResource51	RSC	If bit 19 is set to 1b for local bus node number 51, then asynchronous requests received by the controller from that node are accepted.
18	asynReqResource50	RSC	If bit 18 is set to 1b for local bus node number 50, then asynchronous requests received by the controller from that node are accepted.
17	asynReqResource49	RSC	If bit 17 is set to 1b for local bus node number 49, then asynchronous requests received by the controller from that node are accepted.

Not Recommended for New Designs

Table 8–27. Asynchronous Request Filter High Register Description (Continued)

BIT	FIELD NAME	TYPE	DESCRIPTION
16	asynReqResource48	RSC	If bit 16 is set to 1b for local bus node number 48, then asynchronous requests received by the controller from that node are accepted.
15	asynReqResource47	RSC	If bit 15 is set to 1b for local bus node number 47, then asynchronous requests received by the controller from that node are accepted.
14	asynReqResource46	RSC	If bit 14 is set to 1b for local bus node number 46, then asynchronous requests received by the controller from that node are accepted.
13	asynReqResource45	RSC	If bit 13 is set to 1b for local bus node number 45, then asynchronous requests received by the controller from that node are accepted.
12	asynReqResource44	RSC	If bit 12 is set to 1b for local bus node number 44, then asynchronous requests received by the controller from that node are accepted.
11	asynReqResource43	RSC	If bit 11 is set to 1b for local bus node number 43, then asynchronous requests received by the controller from that node are accepted.
10	asynReqResource42	RSC	If bit 10 is set to 1b for local bus node number 42, then asynchronous requests received by the controller from that node are accepted.
9	asynReqResource41	RSC	If bit 9 is set to 1b for local bus node number 41, then asynchronous requests received by the controller from that node are accepted.
8	asynReqResource40	RSC	If bit 8 is set to 1b for local bus node number 40, then asynchronous requests received by the controller from that node are accepted.
7	asynReqResource39	RSC	If bit 7 is set to 1b for local bus node number 39, then asynchronous requests received by the controller from that node are accepted.
6	asynReqResource38	RSC	If bit 6 is set to 1b for local bus node number 38, then asynchronous requests received by the controller from that node are accepted.
5	asynReqResource37	RSC	If bit 5 is set to 1b for local bus node number 37, then asynchronous requests received by the controller from that node are accepted.
4	asynReqResource36	RSC	If bit 4 is set to 1b for local bus node number 36, then asynchronous requests received by the controller from that node are accepted.
3	asynReqResource35	RSC	If bit 3 is set to 1b for local bus node number 35, then asynchronous requests received by the controller from that node are accepted.
2	asynReqResource34	RSC	If bit 2 is set to 1b for local bus node number 34, then asynchronous requests received by the controller from that node are accepted.
1	asynReqResource33	RSC	If bit 1 is set to 1b for local bus node number 33, then asynchronous requests received by the controller from that node are accepted.
0	asynReqResource32	RSC	If bit 0 is set to 1b for local bus node number 32, then asynchronous requests received by the controller from that node are accepted.

Not Recommended for New Designs

8.36 Asynchronous Request Filter Low Register

The asynchronous request filter low set/clear register enables asynchronous receive requests on a per-node basis, and handles the lower node IDs. Other than filtering different node IDs, this register behaves identically to the asynchronous request filter high register. See Table 8–28 for a complete description of the register contents.

OHCI register offset: 108h set register
10Ch clear register
Register type: Read/Set/Clear
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 8–28. Asynchronous Request Filter Low Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	asynReqResource31	RSC	If bit 31 is set to 1b for local bus node number 31, then asynchronous requests received by the controller from that node are accepted.
30	asynReqResource30	RSC	If bit 30 is set to 1b for local bus node number 30, then asynchronous requests received by the controller from that node are accepted.
29–2	asynReqResourcen	RSC	Bits 29 through 2 (asynReqResourcen, where n = 29, 28, 27, …, 2) follow the same pattern as bits 31 and 30.
1	asynReqResource1	RSC	If bit 1 is set to 1b for local bus node number 1, then asynchronous requests received by the controller from that node are accepted.
0	asynReqResource0	RSC	If bit 0 is set to 1b for local bus node number 0, then asynchronous requests received by the controller from that node are accepted.

Not Recommended for New Designs

8.37 Physical Request Filter High Register

The physical request filter high set/clear register enables physical receive requests on a per-node basis, and handles the upper node IDs. When a packet is destined for the physical request context, and the node ID has been compared against the ARRQ registers, then the comparison is done again with this register. If the bit corresponding to the node ID is not set to 1b in this register, then the request is handled by the ARRQ context instead of the physical request context. The node ID comparison is done if the source node is on the same bus as the controller. Nonlocal bus-sourced packets are not acknowledged unless bit 31 in this register is set to 1b. See Table 8–29 for a complete description of the register contents.

OHCI register offset: 110h set register
114h clear register
Register type: Read/Set/Clear
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 8–29. Physical Request Filter High Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	physReqAllBusses	RSC	If bit 31 is set to 1b, then all asynchronous requests received by the controller from nonlocal bus nodes are accepted. Bit 31 is not cleared by a $\overline{\text{PRST}}$.
30	physReqResource62	RSC	If bit 30 is set to 1b for local bus node number 62, then physical requests received by the controller from that node are handled through the physical request context.
29	physReqResource61	RSC	If bit 29 is set to 1b for local bus node number 61, then physical requests received by the controller from that node are handled through the physical request context.
28	physReqResource60	RSC	If bit 28 is set to 1b for local bus node number 60, then physical requests received by the controller from that node are handled through the physical request context.
27	physReqResource59	RSC	If bit 27 is set to 1b for local bus node number 59, then physical requests received by the controller from that node are handled through the physical request context.
26	physReqResource58	RSC	If bit 26 is set to 1b for local bus node number 58, then physical requests received by the controller from that node are handled through the physical request context.
25	physReqResource57	RSC	If bit 25 is set to 1b for local bus node number 57, then physical requests received by the controller from that node are handled through the physical request context.
24	physReqResource56	RSC	If bit 24 is set to 1b for local bus node number 56, then physical requests received by the controller from that node are handled through the physical request context.
23	physReqResource55	RSC	If bit 23 is set to 1b for local bus node number 55, then physical requests received by the controller from that node are handled through the physical request context.
22	physReqResource54	RSC	If bit 22 is set to 1b for local bus node number 54, then physical requests received by the controller from that node are handled through the physical request context.
21	physReqResource53	RSC	If bit 21 is set to 1b for local bus node number 53, then physical requests received by the controller from that node are handled through the physical request context.
20	physReqResource52	RSC	If bit 20 is set to 1b for local bus node number 52, then physical requests received by the controller from that node are handled through the physical request context.
19	physReqResource51	RSC	If bit 19 is set to 1b for local bus node number 51, then physical requests received by the controller from that node are handled through the physical request context.
18	physReqResource50	RSC	If bit 18 is set to 1b for local bus node number 50, then physical requests received by the controller from that node are handled through the physical request context.
17	physReqResource49	RSC	If bit 17 is set to 1b for local bus node number 49, then physical requests received by the controller from that node are handled through the physical request context.

Not Recommended for New Designs

Table 8–29. Physical Request Filter High Register Description (Continued)

BIT	FIELD NAME	TYPE	DESCRIPTION
16	physReqResource48	RSC	If bit 16 is set to 1b for local bus node number 48, then physical requests received by the controller from that node are handled through the physical request context.
15	physReqResource47	RSC	If bit 15 is set to 1b for local bus node number 47, then physical requests received by the controller from that node are handled through the physical request context.
14	physReqResource46	RSC	If bit 14 is set to 1b for local bus node number 46, then physical requests received by the controller from that node are handled through the physical request context.
13	physReqResource45	RSC	If bit 13 is set to 1b for local bus node number 45, then physical requests received by the controller from that node are handled through the physical request context.
12	physReqResource44	RSC	If bit 12 is set to 1b for local bus node number 44, then physical requests received by the controller from that node are handled through the physical request context.
11	physReqResource43	RSC	If bit 11 is set to 1b for local bus node number 43, then physical requests received by the controller from that node are handled through the physical request context.
10	physReqResource42	RSC	If bit 10 is set to 1b for local bus node number 42, then physical requests received by the controller from that node are handled through the physical request context.
9	physReqResource41	RSC	If bit 9 is set to 1b for local bus node number 41, then physical requests received by the controller from that node are handled through the physical request context.
8	physReqResource40	RSC	If bit 8 is set to 1b for local bus node number 40, then physical requests received by the controller from that node are handled through the physical request context.
7	physReqResource39	RSC	If bit 7 is set to 1b for local bus node number 39, then physical requests received by the controller from that node are handled through the physical request context.
6	physReqResource38	RSC	If bit 6 is set to 1b for local bus node number 38, then physical requests received by the controller from that node are handled through the physical request context.
5	physReqResource37	RSC	If bit 5 is set to 1b for local bus node number 37, then physical requests received by the controller from that node are handled through the physical request context.
4	physReqResource36	RSC	If bit 4 is set to 1b for local bus node number 36, then physical requests received by the controller from that node are handled through the physical request context.
3	physReqResource35	RSC	If bit 3 is set to 1b for local bus node number 35, then physical requests received by the controller from that node are handled through the physical request context.
2	physReqResource34	RSC	If bit 2 is set to 1b for local bus node number 34, then physical requests received by the controller from that node are handled through the physical request context.
1	physReqResource33	RSC	If bit 1 is set to 1b for local bus node number 33, then physical requests received by the controller from that node are handled through the physical request context.
0	physReqResource32	RSC	If bit 0 is set to 1b for local bus node number 32, then physical requests received by the controller from that node are handled through the physical request context.

Not Recommended for New Designs

8.38 Physical Request Filter Low Register

The physical request filter low set/clear register enables physical receive requests on a per-node basis, and handles the lower node IDs. When a packet is destined for the physical request context, and the node ID has been compared against the asynchronous request filter registers, then the node ID comparison is done again with this register. If the bit corresponding to the node ID is not set to 1b in this register, then the request is handled by the asynchronous request context instead of the physical request context. See Table 8–30 for a complete description of the register contents.

OHCI register offset: 118h set register
11Ch clear register
Register type: Read/Set/Clear
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 8–30. Physical Request Filter Low Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	physReqResource31	RSC	If bit 31 is set to 1b for local bus node number 31, then physical requests received by the controller from that node are handled through the physical request context.
30	physReqResource30	RSC	If bit 30 is set to 1b for local bus node number 30, then physical requests received by the controller from that node are handled through the physical request context.
29–2	physReqResourcen	RSC	Bits 29 through 2 (physReqResourcen, where n = 29, 28, 27, …, 2) follow the same pattern as bits 31 and 30.
1	physReqResource1	RSC	If bit 1 is set to 1b for local bus node number 1, then physical requests received by the controller from that node are handled through the physical request context.
0	physReqResource0	RSC	If bit 0 is set to 1b for local bus node number 0, then physical requests received by the controller from that node are handled through the physical request context.

8.39 Physical Upper Bound Register (Optional Register)

The physical upper bound register is an optional register and is not implemented. This register returns 0000 0000h when read.

OHCI register offset: 120h
Register type: Read-only
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Not Recommended for New Designs

8.40 Asynchronous Context Control Register

The asynchronous context control set/clear register controls the state and indicates status of the DMA context. See Table 8–31 for a complete description of the register contents.

OHCI register offset:	180h	set register	[ATRQ]
	184h	clear register	[ATRQ]
	1A0h	set register	[ATRS]
	1A4h	clear register	[ATRS]
	1C0h	set register	[ARRQ]
	1C4h	clear register	[ARRQ]
	1E0h	set register	[ARRS]
	1E4h	clear register	[ARRS]
Register type:	Read/Set/Clear/Update, Read/Set/Update, Read/Update, Read-only		
Default value:	0000 X0XXh		

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	X	0	0	0	0	X	X	X	X	X	X	X	X

Table 8–31. Asynchronous Context Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–16	RSVD	R	Reserved. Bits 31–16 return 0000h when read.
15	run	RSCU	Bit 15 is set to 1b by software to enable descriptor processing for the context and cleared by software to stop descriptor processing. The controller changes this bit only on a system (hardware) or software reset.
14–13	RSVD	R	Reserved. Bits 14 and 13 return 00b when read.
12	wake	RSU	Software sets bit 12 to 1b to cause the controller to continue or resume descriptor processing. The controller clears this bit on every descriptor fetch.
11	dead	RU	The controller sets bit 11 to 1b when it encounters a fatal error, and clears the bit when software clears bit 15 (run). Asynchronous contexts supporting out-of-order pipelining provide unique ContextControl.dead functionality. See Section 7.7 in the *1394 Open Host Controller Interface Specification* (Release 1.1) for more information.
10	active	RU	The controller sets bit 10 to 1b when it is processing descriptors.
9–8	RSVD	R	Reserved. Bits 9 and 8 return 00b when read.
7–5	spd	RU	This field indicates the speed at which a packet was received or transmitted and only contains meaningful information for receive contexts. This field is encoded as: 000 = 100M bits/s 001 = 200M bits/s 010 = 400M bits/s All other values are reserved.
4–0	eventcode	RU	This field holds the acknowledge sent by the link core for this packet or an internally-generated error code if the packet was not transferred successfully.

Not Recommended for New Designs

8.41 Asynchronous Context Command Pointer Register

The asynchronous context command pointer register contains a pointer to the address of the first descriptor block that the controller accesses when software enables the context by setting bit 15 (run) in the asynchronous context control register (see Section 8.40) to 1b. See Table 8–32 for a complete description of the register contents.

OHCI register offset: 18Ch [ATRQ]
1ACh [ATRS]
1CCh [ARRQ]
1ECh [ARRS]
Register type: Read/Write/Update
Default value: XXXX XXXXh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 8–32. Asynchronous Context Command Pointer Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–4	descriptorAddress	RWU	Contains the upper 28 bits of the address of a 16-byte aligned descriptor block.
3–0	Z	RWU	Indicates the number of contiguous descriptors at the address pointed to by the descriptor address. If Z is 0h, then it indicates that the descriptorAddress field (bits 31–4) is not valid.

Not Recommended for New Designs

8.42 Isochronous Transmit Context Control Register

The isochronous transmit context control set/clear register controls options, state, and status for the isochronous transmit DMA contexts. The n value in the following register addresses indicates the context number (n = 0, 1, 2, 3, …, 7). See Table 8–33 for a complete description of the register contents.

OHCI register offset: 200h + (16 * n) set register
204h + (16 * n) clear register
Register type: Read/Set/Clear/Update, Read/Set/Clear, Read/Set/Update, Read/Update, Read-only
Default value: XXXX X0XXh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	X	0	0	0	0	X	X	X	X	X	X	X	X

Table 8–33. Isochronous Transmit Context Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	cycleMatchEnable	RSCU	When bit 31 is set to 1b, processing occurs such that the packet described by the context first descriptor block is transmitted in the cycle whose number is specified in the cycleMatch field (bits 30–16). The cycleMatch field (bits 30–16) must match the low-order two bits of cycleSeconds and the 13-bit cycleCount field in the cycle start packet that is sent or received immediately before isochronous transmission begins. Since the isochronous transmit DMA controller may work ahead, the processing of the first descriptor block may begin slightly in advance of the actual cycle in which the first packet is transmitted. The effects of this bit, however, are impacted by the values of other bits in this register and are explained in the *1394 Open Host Controller Interface Specification.* Once the context has become active, hardware clears this bit.
30–16	cycleMatch	RSC	This field contains a 15-bit value, corresponding to the low-order two bits of the isochronous cycle timer register at OHCI offset F0h (see Section 8.34) cycleSeconds field (bits 31–25) and the cycleCount field (bits 24–12). If bit 31 (cycleMatchEnable) is set to 1b, then this isochronous transmit DMA context becomes enabled for transmits when the low-order two bits of the isochronous cycle timer register at OHCI offset F0h cycleSeconds field (bits 31–25) and the cycleCount field (bits 24–12) value equal this field (cycleMatch) value.
15	run	RSC	Bit 15 is set to 1b by software to enable descriptor processing for the context and cleared by software to stop descriptor processing. The controller changes this bit only on a system (hardware) or software reset.
14–13	RSVD	R	Reserved. Bits 14 and 13 return 00b when read.
12	wake	RSU	Software sets bit 12 to 1b to cause the controller to continue or resume descriptor processing. The controller clears this bit on every descriptor fetch.
11	dead	RU	The controller sets bit 11 to 1b when it encounters a fatal error, and clears the bit when software clears bit 15 (run) to 0b.
10	active	RU	The controller sets bit 10 to 1b when it is processing descriptors.
9–8	RSVD	R	Reserved. Bits 9 and 8 return 00b when read.
7–5	spd	RU	This field in not meaningful for isochronous transmit contexts.
4–0	event code	RU	Following an OUTPUT_LAST* command, the error code is indicated in this field. Possible values are: ack_complete, evt_descriptor_read, evt_data_read, and evt_unknown.

† On an overflow for each running context, the isochronous transmit DMA supports up to 7 cycle skips, when the following are true:
1. Bit 11 (dead) in either the isochronous transmit or receive context control register is set to 1b.
2. Bits 4–0 (eventcode field) in either the isochronous transmit or receive context control register are set to evt_timeout.
3. Bit 24 (unrecoverableError) in the interrupt event register at OHCI offset 80h/84h (see Section 8.21) is set to 1b.

Not Recommended for New Designs

8.43 Isochronous Transmit Context Command Pointer Register

The isochronous transmit context command pointer register contains a pointer to the address of the first descriptor block that the controller accesses when software enables an isochronous transmit context by setting bit 15 (run) in the isochronous transmit context control register (see Section 8.42) to 1b. The isochronous transmit DMA context command pointer can be read when a context is active. The n value in the following register addresses indicates the context number (n = 0, 1, 2, 3, …, 7).

OHCI register offset: 20Ch + (16 * n)
Register type: Read-only
Default value: XXXX XXXXh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

8.44 Isochronous Receive Context Control Register

The isochronous receive context control set/clear register controls options, state, and status for the isochronous receive DMA contexts. The n value in the following register addresses indicates the context number (n = 0, 1, 2, 3). See Table 8–34 for a complete description of the register contents.

OHCI register offset: 400h + (32 * n) set register
404h + (32 * n) clear register
Register type: Read/Set/Clear/Update, Read/Set/Clear, Read/Set/Update, Read/Update, Read-only
Default value: XX00 X0XXh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	X	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	X	0	0	0	0	X	X	X	X	X	X	X	X

Table 8–34. Isochronous Receive Context Control Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	bufferFill	RSC	When bit 31 is set to 1b, received packets are placed back-to-back to completely fill each receive buffer. When this bit is cleared, each received packet is placed in a single buffer. If bit 28 (multiChanMode) is set to 1b, then this bit must also be set to 1b. The value of this bit must not be changed while bit 10 (active) or bit 15 (run) is set to 1b.
30	isochHeader	RSC	When bit 30 is set to 1b, received isochronous packets include the complete 4-byte isochronous packet header seen by the link layer. The end of the packet is marked with a xferStatus in the first doublet, and a 16-bit timeStamp indicating the time of the most recently received (or sent) cycleStart packet. When this bit is cleared, the packet header is stripped from received isochronous packets. The packet header, if received, immediately precedes the packet payload. The value of this bit must not be changed while bit 10 (active) or bit 15 (run) is set to 1b.
29	cycleMatchEnable	RSCU	When bit 29 is set to 1b and the 13-bit cycleMatch field (bits 24–12) in the isochronous receive context match register (See Section 8.46) matches the 13-bit cycleCount field in the cycleStart packet, the context begins running. The effects of this bit, however, are impacted by the values of other bits in this register. Once the context has become active, hardware clears this bit. The value of this bit must not be changed while bit 10 (active) or bit 15 (run) is set to 1b.

Not Recommended for New Designs

Table 8–34. Isochronous Receive Context Control Register Description (Continued)

BIT	FIELD NAME	TYPE	DESCRIPTION
28	multiChanMode	RSC	When bit 28 is set to 1b, the corresponding isochronous receive DMA context receives packets for all isochronous channels enabled in the isochronous receive channel mask high register at OHCI offset 70h/74h (see Section 8.19) and isochronous receive channel mask low register at OHCI offset 78h/7Ch (see Section 8.20). The isochronous channel number specified in the isochronous receive context match register (see Section 8.46) is ignored. When this bit is cleared, the isochronous receive DMA context receives packets for the single channel specified in the isochronous receive context match register (see Section 8.46). Only one isochronous receive DMA context may use the isochronous receive channel mask registers (see Sections 8.19, and 8.20). If more than one isochronous receive context control register has this bit set, then the results are undefined. The value of this bit must not be changed while bit 10 (active) or bit 15 (run) is set to 1b.
27	dualBufferMode	RSC	When bit 27 is set to 1b, receive packets are separated into first and second payload and streamed independently to the firstBuffer series and secondBuffer series as described in Section 10.2.3 in the *1394 Open Host Controller Interface Specification*. Also, when bit 27 is set to 1b, both bits 28 (multiChanMode) and 31 (bufferFill) are cleared to 00b. The value of this bit does not change when either bit 10 (active) or bit 15 (run) is set to 1b.
26–16	RSVD	R	Reserved. Bits 26–16 return 000 0000 0000b when read.
15	run	RSCU	Bit 15 is set to 1b by software to enable descriptor processing for the context and cleared by software to stop descriptor processing. The controller changes this bit only on a system (hardware) or software reset.
14–13	RSVD	R	Reserved. Bits 14 and 13 return 00b when read.
12	wake	RSU	Software sets bit 12 to 1b to cause the controller to continue or resume descriptor processing. The controller clears this bit on every descriptor fetch.
11	dead	RU	The controller sets bit 11 to 1b when it encounters a fatal error, and clears the bit when software clears bit 15 (run).
10	active	RU	The controller sets bit 10 to 1b when it is processing descriptors.
9–8	RSVD	R	Reserved. Bits 9 and 8 return 00b when read.
7–5	spd	RU	This field indicates the speed at which the packet was received. 000 = 100M bits/s 001 = 200M bits/s 010 = 400M bits/s All other values are reserved.
4–0	event code	RU	For bufferFill mode, possible values are: ack_complete, evt_descriptor_read, evt_data_write, and evt_unknown. Packets with data errors (either dataLength mismatches or dataCRC errors) and packets for which a FIFO overrun occurred are backed out. For packet-per-buffer mode, possible values are: ack_complete, ack_data_error, evt_long_packet, evt_overrun, evt_descriptor_read, evt_data_write, and evt_unknown.

8.45 Isochronous Receive Context Command Pointer Register

The isochronous receive context command pointer register contains a pointer to the address of the first descriptor block that the controller accesses when software enables an isochronous receive context by setting bit 15 (run) in the isochronous receive context control register (see Section 8.44) to 1b. The n value in the following register addresses indicates the context number (n = 0, 1, 2, 3).

OHCI register offset: 40Ch + (32 * n)
Register type: Read-only
Default value: XXXX XXXXh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Not Recommended for New Designs

8.46 Isochronous Receive Context Match Register

The isochronous receive context match register starts an isochronous receive context running on a specified cycle number, filters incoming isochronous packets based on tag values, and waits for packets with a specified sync value. The n value in the following register addresses indicates the context number (n = 0, 1, 2, 3). See Table 8–35 for a complete description of the register contents.

OHCI register offset: 410h + (32 * n)
Register type: Read/Write, Read-only
Default value: XXXX XXXXh

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X

Table 8–35. Isochronous Receive Context Match Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	tag3	RW	If bit 31 is set to 1b, then this context matches on isochronous receive packets with a tag field of 11b.
30	tag2	RW	If bit 30 is set to 1b, then this context matches on isochronous receive packets with a tag field of 10b.
29	tag1	RW	If bit 29 is set to 1b, then this context matches on isochronous receive packets with a tag field of 01b.
28	tag0	RW	If bit 28 is set to 1b, then this context matches on isochronous receive packets with a tag field of 00b.
27	RSVD	R	Reserved. Bit 27 returns 0b when read.
26–12	cycleMatch	RW	This field contains a 15-bit value corresponding to the two low-order bits of cycleSeconds and the 13-bit cycleCount field in the cycleStart packet. If cycleMatchEnable (bit 29) in the isochronous receive context control register (see Section 8.44) is set to 1b, then this context is enabled for receives when the two low-order bits of the isochronous cycle timer register at OHCI offset F0h (see Section 8.34) cycleSeconds field (bits 31–25) and cycleCount field (bits 24–12) value equal this field (cycleMatch) value.
11–8	sync	RW	This 4-bit field is compared to the sync field of each isochronous packet for this channel when the command descriptor w field is set to 11b.
7	RSVD	R	Reserved. Bit 7 returns 0b when read.
6	tag1SyncFilter	RW	If bit 6 and bit 29 (tag1) are set to 11b, then packets with tag 01b are accepted into the context if the two most significant bits of the packet sync field are 00b. Packets with tag values other than 01b are filtered according to bit 28 (tag0), bit 30 (tag2), and bit 31 (tag3) without any additional restrictions. If this bit is cleared, then this context matches on isochronous receive packets as specified in bits 28–31 (tag0–tag3) with no additional restrictions.
5–0	channelNumber	RW	This 6-bit field indicates the isochronous channel number for which this isochronous receive DMA context accepts packets.

Not Recommended for New Designs

9 1394 OHCI Memory-Mapped TI Extension Register Space

The TI extension base address register provides a method of accessing memory-mapped TI extension registers. See Section 7.9, *TI Extension Base Address Register*, for register bit field details. See Table 9–1 for the TI extension register listing.

Table 9–1. TI Extension Register Map

REGISTER NAME	OFFSET
Reserved	00h–A7Fh
Isochronous Receive DV Enhancement Set	A80h
Isochronous Receive DV Enhancement Clear	A84h
Link Enhancement Control Set	A88h
Link Enhancement Control Clear	A8Ch
Isochronous Transmit Context 0 Timestamp Offset	A90h
Isochronous Transmit Context 1 Timestamp Offset	A94h
Isochronous Transmit Context 2 Timestamp Offset	A98h
Isochronous Transmit Context 3 Timestamp Offset	A9Ch
Isochronous Transmit Context 4 Timestamp Offset	AA0h
Isochronous Transmit Context 5 Timestamp Offset	AA4h
Isochronous Transmit Context 6 Timestamp Offset	AA8h
Isochronous Transmit Context 7 Timestamp Offset	AACh

9.1 DV and MPEG2 Timestamp Enhancements

The DV timestamp enhancements are enabled by bit 8 (enab_dv_ts) in the link enhancement control register located at PCI offset F4h and are aliased in TI extension register space at offset A88h (set) and A8Ch (clear).

The DV and MPEG transmit enhancements are enabled separately by bits in the link enhancement control register located in PCI configuration space at PCI offset F4h. The link enhancement control register is also aliased as a set/clear register in TI extension space at offset A88h (set) and A8Ch (clear).

Bit 8 (enab_dv_ts) of the link enhancement control register enables DV timestamp support. When enabled, the link calculates a timestamp based on the cycle timer and the timestamp offset register and substitutes it in the SYT field of the CIP once per DV frame.

Bit 10 (enab_mpeg_ts) of the link enhancement control register enables MPEG timestamp support. Two MPEG time stamp modes are supported. The default mode calculates an initial delta that is added to the calculated timestamp in addition to a user-defined offset. The initial offset is calculated as the difference in the intended transmit cycle count and the cycle count field of the timestamp in the first TSP of the MPEG2 stream. The use of the initial delta can be controlled by bit 31 (DisableInitialOffset) in the timestamp offset register (see Section 9.5).

The MPEG2 timestamp enhancements are enabled by bit 10 (enab_mpeg_ts) in the link enhancement control register located at PCI offset F4h and aliased in TI extension register space at offset A88h (set) and A8Ch (clear).

When bit 10 (enab_mpeg_ts) is set to 1b, the hardware applies the timestamp enhancements to isochronous transmit packets that have the tag field equal to 01b in the isochronous packet header and a FMT field equal to 10h.

Not Recommended for New Designs

9.2 Isochronous Receive Digital Video Enhancements

The DV frame sync and branch enhancement provides a mechanism in buffer-fill mode to synchronize 1394 DV data that is received in the correct order to DV frame-sized data buffers described by several INPUT_MORE descriptors (see *1394 Open Host Controller Interface Specification*, Release 1.1). This is accomplished by waiting for the start-of-frame packet in a DV stream before transferring the received isochronous stream into the memory buffer described by the INPUT_MORE descriptors. This can improve the DV capture application performance by reducing the amount of processing overhead required to strip the CIP header and copy the received packets into frame-sized buffers.

The start of a DV frame is represented in the 1394 packet as a 16-bit pattern of 1FX7h (first byte 1Fh and second byte X7h) received as the first two bytes of the third quadlet in a DV isochronous packet.

9.3 Isochronous Receive Digital Video Enhancements Register

The isochronous receive digital video enhancements register enables the DV enhancements in the controller. The bits in this register may only be modified when both the active (bit 10) and run (bit 15) bits of the corresponding context control register are 00b. See Table 9–2 for a complete description of the register contents.

TI extension register offset: A80h set register
A84h clear register
Register type: Read/Set/Clear, Read-only
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 9–2. Isochronous Receive Digital Video Enhancements Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–14	RSVD	R	Reserved. Bits 31–14 return 00 0000 0000 0000 0000b when read.
13	DV_Branch3	RSC	When bit 13 is set to 1b, the isochronous receive context 3 synchronizes reception to the DV frame start tag in bufferfill mode if input_more.b = 01b, and jumps to the descriptor pointed to by frameBranch if a DV frame start tag is received out of place. This bit is only interpreted when bit 12 (CIP_Strip3) is set to 1b and bit 30 (isochHeader) in the isochronous receive context control register at OHCI offset 460h/464h (see Section 8.44) is cleared to 0b.
12	CIP_Strip3	RSC	When bit 12 is set to 1b, the isochronous receive context 3 strips the first two quadlets of payload. This bit is only interpreted when bit 30 (isochHeader) in the isochronous receive context control register at OHCI offset 460h/464h (see Section 8.44) is cleared to 0b.
11–10	RSVD	R	Reserved. Bits 11 and 10 return 00b when read.
9	DV_Branch2	RSC	When bit 9 is set to 1b, the isochronous receive context 2 synchronizes reception to the DV frame start tag in bufferfill mode if input_more.b = 01b, and jumps to the descriptor pointed to by frameBranch if a DV frame start tag is received out of place. This bit is only interpreted when bit 8 (CIP_Strip2) is set to 1b and bit 30 (isochHeader) in the isochronous receive context control register at OHCI offset 440h/444h (see Section 8.44) is cleared to 0b.
8	CIP_Strip2	RSC	When bit 8 is set to 1b, the isochronous receive context 2 strips the first two quadlets of payload. This bit is only interpreted when bit 30 (isochHeader) in the isochronous receive context control register at OHCI offset 440h/444h (see Section 8.44) is cleared to 0b.
7–6	RSVD	R	Reserved. Bits 7 and 6 return 00b when read.

Not Recommended for New Designs

Table 9–2. Isochronous Receive Digital Video Enhancements Register Description (Continued)

BIT	FIELD NAME	TYPE	DESCRIPTION
5	DV_Branch1	RSC	When bit 5 is set to 1b, the isochronous receive context 1 synchronizes reception to the DV frame start tag in bufferfill mode if input_more.b = 01b, and jumps to the descriptor pointed to by frameBranch if a DV frame start tag is received out of place. This bit is only interpreted when bit 4 (CIP_Strip1) is set to 1b and bit 30 (isochHeader) in the isochronous receive context control register at OHCI offset 420h/424h (see Section 8.44) is cleared to 0b.
4	CIP_Strip1	RSC	When bit 4 is set to 1b, the isochronous receive context 1 strips the first two quadlets of payload. This bit is only interpreted when bit 30 (isochHeader) in the isochronous receive context control register at OHCI offset 420h/424h (see Section 8.44) is cleared to 0b.
3–2	RSVD	R	Reserved. Bits 3 and 2 return 00b when read.
1	DV_Branch0	RSC	When bit 1 is set to 1b, the isochronous receive context 0 synchronizes reception to the DV frame start tag in bufferfill mode if input_more.b = 01b and jumps to the descriptor pointed to by frameBranch if a DV frame start tag is received out of place. This bit is only interpreted when bit 0 (CIP_Strip0) is set to 1b and bit 30 (isochHeader) in the isochronous receive context control register at OHCI offset 400h/404h (see Section 8.44) is cleared to 0b.
0	CIP_Strip0	RSC	When bit 0 is set to 1b, the isochronous receive context 0 strips the first two quadlets of payload. This bit is only interpreted when bit 30 (isochHeader) in the isochronous receive context control register at OHCI offset 400h/404h (see Section 8.44) is cleared to 0b.

9.4 Link Enhancement Register

This register is a memory-mapped set/clear register that is an alias of the link enhancement control register at PCI offset F4h. These bits may be initialized by software. Some of the bits may also be initialized by a serial EEPROM, if one is present, as noted in the bit descriptions below. If the bits are to be initialized by software, then the bits must be initialized prior to setting bit 19 (LPS) in the host controller control register at OHCI offset 50h/54h (see Section 8.16). See Table 9–3 for a complete description of the register contents.

TI extension register offset: A88h set register
A8Ch clear register
Register type: Read/Set/Clear, Read-only
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Table 9–3. Link Enhancement Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31–16	RSVD	R	Reserved. Bits 31–16 return 0000h when read.
15†	dis_at_pipeline	RW	Disable AT pipelining. When bit 15 is set to 1b, out-of-order AT pipelining is disabled. The default value for this bit is 0b.
14†	RSVD	RW	Reserved. Bit 14 defaults to 0b and must remain 0b for normal operation of the OHCI core.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Not Recommended for New Designs

Table 9–3. Link Enhancement Register Description (Continued)

BIT	FIELD NAME	TYPE	DESCRIPTION
13–12†	atx_thresh	RW	This field sets the initial AT threshold value, which is used until the AT FIFO is underrun. When the OHCI controller retries the packet, it uses a 2K-byte threshold, resulting in a store-and-forward operation. 00 = Threshold ~ 2K bytes resulting in a store-and-forward operation 01 = Threshold ~ 1.7K bytes (default) 10 = Threshold ~ 1K bytes 11 = Threshold ~ 512 bytes These bits fine-tune the asynchronous transmit threshold. For most applications the 1.7K-byte threshold is optimal. Changing this value may increase or decrease the 1394 latency depending on the average PCI bus latency. Setting the AT threshold to 1.7K, 1K, or 512 bytes results in data being transmitted at these thresholds or when an entire packet has been checked into the FIFO. If the packet to be transmitted is larger than the AT threshold, then the remaining data must be received before the AT FIFO is emptied; otherwise, an underrun condition occurs, resulting in a packet error at the receiving node. As a result, the link then commences store-and-forward operation. Wait until it has the complete packet in the FIFO before retransmitting it on the second attempt to ensure delivery. An AT threshold of 2K results in store-and-forward operation, which means that asynchronous data will not be transmitted until an end-of-packet token is received. Restated, setting the AT threshold to 2K results in only complete packets being transmitted. Note that the OHCI controller will always use store-and-forward when the asynchronous transmit retries register at OHCI offset 08h (see Section 8.3, *Asynchronous Transmit Retries Register*) is cleared.
11	RSVD	R	Reserved. Bit 11 returns 0b when read.
10†	enab_mpeg_ts	RW	Enable MPEG CIP timestamp enhancement. When bit 9 is set to 1b, the enhancement is enabled for MPEG CIP transmit streams (FMT = 20h). The default value for this bit is 0b.
9	RSVD	R	Reserved. Bit 9 returns 0b when read.
8†	enab_dv_ts	RW	Enable DV CIP timestamp enhancement. When bit 8 is set to 1b, the enhancement is enabled for DV CIP transmit streams (FMT = 00h). The default value for this bit is 0b.
7†	enab_unfair	RW	Enable asynchronous priority requests. OHCI-Lynx™ compatible. Setting bit 7 to 1b enables the link to respond to requests with priority arbitration. It is recommended that this bit be set to 1b. The default value for this bit is 0b.
6–3	RSVD	R	Reserved. Bits 6–3 return 0h when read.
2†	RSVD	RW	Reserved. Bit 2 defaults to 0b and must remain 0b for normal operation of the OHCI core.
1†	enab_accel	RW	Enable acceleration enhancements. OHCI-Lynx™ compatible. When bit 1 is set to 1b, the PHY layer is notified that the link supports the IEEE Std 1394a-2000 acceleration enhancements, that is, ack-accelerated, fly-by concatenation, etc. It is recommended that this bit be set to 1b. The default value for this bit is 0b.
0	RSVD	R	Reserved. Bit 0 returns 0b when read.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Not Recommended for New Designs

9.5 Timestamp Offset Register

The value of this register is added as an offset to the cycle timer value when using the MPEG, DV, and CIP enhancements. A timestamp offset register is implemented per isochronous transmit context. The n value following the offset indicates the context number (n = 0, 1, 2, 3, …, 7). These registers are programmed by software as appropriate. See Table 9–4 for a complete description of the register contents.

TI extension register offset: A90h + (4*n)
Register type: Read/Write, Read-only
Default value: 0000 0000h

BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT NUMBER	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET STATE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 9–4. Timestamp Offset Register Description

BIT	FIELD NAME	TYPE	DESCRIPTION
31	DisableInitialOffset	RW	Bit 31 disables the use of the initial timestamp offset when the MPEG2 enhancements are enabled. A value of 0b indicates the use of the initial offset, a value of 1b indicates that the initial offset must not be applied to the calculated timestamp. This bit has no meaning for the DV timestamp enhancements. The default value for this bit is 0b.
30–25	RSVD	R	Reserved. Bits 30–25 return 000 0000b when read.
24–12	CycleCount	RW	This field adds an offset to the cycle count field in the timestamp when the DV or MPEG2 enhancements are enabled. The cycle count field is incremented modulo 8000; therefore, values in this field must be limited between 0 and 7999. The default value for this field is all 0s.
11–0	CycleOffset	RW	This field adds an offset to the cycle offset field in the timestamp when the DV or MPEG2 enhancements are enabled. The cycle offset field is incremented modulo 3072; therefore, values in this field must be limited between 0 and 3071. The default value for this field is all 0s.

Not Recommended for New Designs

10 1394 PHY Configuration Space

There are 16 accessible internal registers in the controller. The configuration of the registers at addresses 0h through 7h (the base registers) is fixed, whereas the configuration of the registers at addresses 8h through Fh (the paged registers) is dependent upon which 1 of 8 pages, numbered 0h through 7h, is currently selected. The selected page is set in base register 7h.

10.1 Base Registers

Table 10−1 shows the configuration of the base registers, and Table 10−2 shows the corresponding field descriptions. The base register field definitions are unaffected by the selected page number.

A reserved register or register field (marked as Reserved in the following register configuration tables) is read as 0, but is subject to future usage. All registers in address pages 2 through 6 are reserved.

Table 10−1. Base Register Configuration

ADDRESS	BIT POSITION							
	0	1	2	3	4	5	6	7
0000	Physical ID						R	CPS
0001	RHB	IBR	Gap_Count					
0010	Extended (111b)			Reserved	Total_Ports (0010b)			
0011	Max_Speed (010b)			Reserved	Delay (0000b)			
0100	LCtrl	C	Jitter (000b)			Pwr_Class		
0101	Watchdog	ISBR	Loop	Pwr_fail	Timeout	Port_event	Enab_accel	Enab_multi
0110	Reserved							
0111	Page_Select			Reserved	Port_Select			

Not Recommended for New Designs

Table 10–2. Base Register Field Descriptions

FIELD	SIZE	TYPE	DESCRIPTION
Physical ID	6	R	This field contains the physical address ID of this node determined during self-ID. The physical ID is invalid after a bus reset until self-ID has completed as indicated by an unsolicited register-0 status transfer.
R	1	R	Root. This bit indicates that this node is the root node. The R bit is cleared to 0b by bus reset and is set to 1b during tree-ID if this node becomes root.
CPS	1	R	Cable-power-status. This bit indicates the state of the CPS input terminal. The CPS terminal is normally tied to serial bus cable power through a 400-kΩ resistor. A 0b in this bit indicates that the cable power voltage has dropped below its threshold for ensured reliable operation.
RHB	1	RW	Root-holdoff bit. This bit instructs the PHY layer to attempt to become root after the next bus reset. The RHB bit is cleared to 0b by a system (hardware) reset and is unaffected by a bus reset.
IBR	1	RW	Initiate bus reset. This bit instructs the PHY layer to initiate a long (166 µs) bus reset at the next opportunity. Any receive or transmit operation in progress when this bit is set completes before the bus reset is initiated. The IBR bit is cleared to 0b after a system (hardware) reset or a bus reset.
Gap_Count	6	RW	Arbitration gap count. This value sets the subaction (fair) gap, arb-reset gap, and arb-delay times. The gap count can be set either by a write to the register, or by reception or transmission of a PHY_CONFIG packet. The gap count is reset to 3Fh by system (hardware) reset or after two consecutive bus resets without an intervening write to the gap count register (either by a write to the PHY register or by a PHY_CONFIG packet).
Extended	3	R	Extended register definition. For the controller, this field is 111b, indicating that the extended register set is implemented.
Total_Ports	4	R	Number of ports. This field indicates the number of ports implemented in the PHY layer. For the controller this field is 2.
Max_Speed	3	R	PHY speed capability. For the PHY layer this field is 010b, indicating S400 speed capability.
Delay	4	R	PHY repeater data delay. This field indicates the worst case repeater data delay of the PHY layer, expressed as 144+(delay × 20) ns. For the controller this field is 0h.
LCtrl	1	RW	Link-active status control. This bit controls the active status of the LLC as indicated during self-ID. The logical AND of this bit and the LPS active status is replicated in the L field (bit 9) of the self-ID packet. The LLC is considered active only if both the LPS input is active and the LCtrl bit is set. The LCtrl bit provides a software controllable means to indicate the LLC active/status in lieu of using the LPS input. The LCtrl bit is set to 1b by a system (hardware) reset and is unaffected by a bus reset. **Note:** The state of the PHY-LLC interface is controlled solely by the LPS input, regardless of the state of the LCtrl bit. If the PHY-LLC interface is operational as determined by the LPS input being active, then received packets and status information continue to be presented on the interface, and any requests indicated on the LREQ input are processed, even if the LCtrl bit is cleared to 0b.
C	1	RW	Contender status. This bit indicates that this node is a contender for the bus or isochronous resource manager. This bit is replicated in the c field (bit 20) of the self-ID packet.
Jitter	3	R	PHY repeater jitter. This field indicates the worst case difference between the fastest and slowest repeater data delay, expressed as (Jitter+1) × 20 ns. For the controller, this field is 000b.
Pwr_Class†	3	RW	Node power class. This field indicates this node power consumption and source characteristics and is replicated in the pwr field (bits 21–23) of the self-ID packet. This field is reset to the state specified by the PC0–PC2 input terminals upon a system (hardware) reset and is unaffected by a bus reset. See Table 10–9.
Watchdog	1	RW	Watchdog enable. This bit, if set to 1b, enables the port event interrupt (Port_event) bit to be set whenever resume operations begin on any port. This bit is cleared to 0b by system (hardware) reset and is unaffected by bus reset.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Not Recommended for New Designs

Table 10–2. Base Register Field Descriptions (Continued)

FIELD	SIZE	TYPE	DESCRIPTION
ISBR	1	RW	Initiate short arbitrated bus reset. This bit, if set to 1b, instructs the PHY layer to initiate a short (1.3 µs) arbitrated bus reset at the next opportunity. This bit is cleared to 0b by a bus reset. **Note:** Legacy IEEE Std 1394-1995 compliant PHY layers can not be capable of performing short bus resets. Therefore, initiation of a short bus reset in a network that contains such a legacy device results in a long bus reset being performed.
Loop	1	RW	Loop detect. This bit is set to 1b when the arbitration controller times out during tree-ID start and may indicate that the bus is configured in a loop. This bit is cleared to 0b by system (hardware) reset or by writing a 1b to this register bit. If the Loop and Watchdog bits are both set and the LLC is or becomes inactive, then the PHY layer activates the LLC to service the interrupt. **Note:** If the network is configured in a loop, then only those nodes which are part of the loop generate a configuration-timeout interrupt. All other nodes instead time out waiting for the tree-ID and/or self-ID process to complete and then generate a state time-out interrupt and bus-reset.
Pwr_fail	1	RW	Cable power failure detect. This bit is set to 1b whenever the CPS input transitions from high to low indicating that cable power may be too low for reliable operation. This bit is cleared to 0b by system (hardware) reset or by writing a 1b to this register bit.
Timeout	1	RW	State time-out interrupt. This bit indicates that a state time-out has occurred (which also causes a bus reset to occur). This bit is cleared to 0b by system (hardware) reset or by writing a 1b to this register bit.
Port_event	1	RW	Port event detect. This bit is set to 1b upon a change in the bias (unless disabled) connected, disabled, or fault bits for any port for which the port interrupt enable (Int_enable) bit is set. Additionally, if the Watchdog bit is set, then the Port_event bit is set to 1b at the start of resume operations on any port. This bit is cleared to 0b by system (hardware) reset or by writing a 1b to this register bit.
Enab_accel	1	RW	Enable accelerated arbitration. This bit enables the PHY layer to perform the various arbitration acceleration enhancements defined in IEEE Std 1394a-2000 (ACK-accelerated arbitration, asynchronous fly-by concatenation, and isochronous fly-by concatenation). This bit is cleared to 0b by system (hardware) reset and is unaffected by bus reset.
Enab_multi	1	RW	Enable multispeed concatenated packets. This bit enables the PHY layer to transmit concatenated packets of differing speeds in accordance with the protocols defined in IEEE Std 1394a-2000. This bit is cleared to 0b by system (hardware) reset and is unaffected by bus reset.
Page_Select	3	RW	Page_Select. This field selects the register page to use when accessing register addresses 8 through 15. This field is cleared to 000b by a system (hardware) reset and is unaffected by bus reset.
Port_Select	4	RW	Port_Select. This field selects the port when accessing per-port status or control (for example, when one of the port status/control registers is accessed in page 0). Ports are numbered starting at 0. This field is cleared to 0h by system (hardware) reset and is unaffected by bus reset.

† These bits are reset by a PCI Express reset ($\overline{\text{PERST}}$), a $\overline{\text{GRST}}$, or the internally-generated power-on reset.

Not Recommended for New Designs

10.2 Port Status Register

The port status page provides access to configuration and status information for each of the ports. The port is selected by writing 0 to the Page_Select field and the desired port number to the Port_Select field in base register 7. Table 10–3 shows the configuration of the port status page registers and Table 10–4 shows the corresponding field descriptions. If the selected port is not implemented, then all registers in the port status page are read as 0.

Table 10–3. Page 0 (Port Status) Register Configuration

ADDRESS	BIT POSITION							
	0	1	2	3	4	5	6	7
1000	AStat		BStat		Ch	Con	Bias	Dis
1001	Peer_Speed			Int_enable	Fault	Reserved		
1010	Reserved							
1011	Reserved							
1100	Reserved							
1101	Reserved							
1110	Reserved							
1111	Reserved							

Table 10–4. Page 0 (Port Status) Register Field Descriptions

FIELD	SIZE	TYPE	DESCRIPTION
AStat	2	R	TPA line state. This field indicates the TPA line state of the selected port, encoded as follows: Code — Arb Value 11 — Z 10 — 0 01 — 1 00 — invalid
BStat	2	R	TPB line state. This field indicates the TPB line state of the selected port. This field has the same encoding as the AStat field.
Ch	1	R	Child/parent status. A 1b indicates that the selected port is a child port. A 0b indicates that the selected port is the parent port. A disconnected, disabled, or suspended port is reported as a child port. The Ch bit is invalid after a bus reset until tree-ID has completed.
Con	1	R	Debounced port connection status. This bit indicates that the selected port is connected. The connection must be stable for the debounce time of approximately 341 ms for the Con bit to be set to 1b. The Con bit is cleared to 0b by system (hardware) reset and is unaffected by bus reset. **Note:** The Con bit indicates that the port is physically connected to a peer PHY device, but the port is not necessarily active.
Bias	1	R	Debounced incoming cable bias status. A 1b indicates that the selected port is detecting incoming cable bias. The incoming cable bias must be stable for the debounce time of 52 µs for the Bias bit to be set to 1b.
Dis	1	RW	Port disabled control. If the Dis bit is set to 1b, then the selected port is disabled. The Dis bit is cleared to 0b by system (hardware) reset (all ports are enabled for normal operation following system (hardware) reset). The Dis bit is not affected by bus reset.
Peer_Speed	3	R	Port peer speed. This field indicates the highest speed capability of the peer PHY device connected to the selected port, encoded as follows: Code — Peer Speed 000 — S100 001 — S200 010 — S400 011–111 — invalid The Peer_Speed field is invalid after a bus reset until self-ID has completed. **Note:** Peer speed codes higher than 010b (S400) are defined in IEEE Std 1394a-2000. However, the controller is only capable of detecting peer speeds up to S400.

Not Recommended for New Designs

Table 10–4. Page 0 (Port Status) Register Field Descriptions (Continued)

FIELD	SIZE	TYPE	DESCRIPTION
Int_enable	1	RW	Port event interrupt enable. When the Int_enable bit is set to 1b, a port event on the selected port sets the port event interrupt (Port_event) bit and notifies the link. This bit is cleared to 0b by a system (hardware) reset and is unaffected by bus reset.
Fault	1	RW	Fault. This bit indicates that a resume-fault or suspend-fault has occurred on the selected port, and that the port is in the suspended state. A resume-fault occurs when a resuming port fails to detect incoming cable bias from its attached peer. A suspend-fault occurs when a suspending port continues to detect incoming cable bias from its attached peer. Writing 1b to this bit clears the fault bit to 0b. This bit is cleared to 0b by system (hardware) reset and is unaffected by bus reset.

10.3 Vendor Identification Register

The vendor identification page identifies the vendor/manufacturer and compliance level. The page is selected by writing 1 to the Page_Select field in base register 7. Table 10–5 shows the configuration of the vendor identification page, and Table 10–6 shows the corresponding field descriptions.

Table 10–5. Page 1 (Vendor ID) Register Configuration

ADDRESS	BIT POSITION							
	0	1	2	3	4	5	6	7
1000	Compliance							
1001	Reserved							
1010	Vendor_ID[0]							
1011	Vendor_ID[1]							
1100	Vendor_ID[2]							
1101	Product_ID[0]							
1110	Product_ID[1]							
1111	Product_ID[2]							

Table 10–6. Page 1 (Vendor ID) Register Field Descriptions

FIELD	SIZE	TYPE	DESCRIPTION
Compliance	8	R	Compliance level. For the controller this field is 01h, indicating compliance with IEEE Std 1394a-2000.
Vendor_ID	24	R	Manufacturer's organizationally unique identifier (OUI). For the controller this field is 08 0028h (Texas Instruments) (the MSB is at register address 1010b).
Product_ID	24	R	Product identifier. For the controller this field is 42 4499h (the MSB is at register address 1101b).

Not Recommended for New Designs

10.4 Vendor-Dependent Register

The vendor-dependent page provides access to the special control features of the controller, as well as to configuration and status information used in manufacturing test and debug. This page is selected by writing 7 to the Page_Select field in base register 7. Table 10–7 shows the configuration of the vendor-dependent page, and Table 10–8 shows the corresponding field descriptions.

Table 10–7. Page 7 (Vendor-Dependent) Register Configuration

ADDRESS	BIT POSITION							
	0	1	2	3	4	5	6	7
1000	NPA	Reserved					Link_Speed	
1001	Reserved for test							
1010	Reserved for test							
1011	Reserved for test							
1100	Reserved for test							
1101	Reserved for test							
1110	Reserved for test							
1111	Reserved for test							

Table 10–8. Page 7 (Vendor-Dependent) Register Field Descriptions

FIELD	SIZE	TYPE	DESCRIPTION
NPA	1	RW	Null-packet actions flag. This bit instructs the PHY layer to not clear fair and priority requests when a null packet is received with arbitration acceleration enabled. If this bit is set to 1b, then fair and priority requests are cleared only when a packet of more than 8 bits is received; ACK packets (exactly 8 data bits), null packets (no data bits), and malformed packets (less than 8 data bits) do not clear fair and priority requests. If this bit is cleared to 0b, then fair and priority requests are cleared when any non-ACK packet is received, including null packets or malformed packets of less than 8 bits. This bit is cleared to 0b by system (hardware) reset and is unaffected by bus reset.
Link_Speed	2	RW	Link speed. This field indicates the top speed capability of the attached LLC. Encoding is as follows: Code — Speed 00 — S100 01 — S200 10 — S400 11 — illegal This field is replicated in the sp field of the self-ID packet to indicate the speed capability of the node (PHY and LLC in combination). However, this field does not affect the PHY speed capability indicated to peer PHYs during self-ID; the PHY layer identifies itself as S400 capable to its peers regardless of the value in this field. This field is set to 10b (S400) by system (hardware) reset and is unaffected by bus reset.

10.5 Power-Class Programming

The PC0–PC2 terminals are programmed to set the default value of the power-class indicated in the pwr field (bits 21–23) of the transmitted self-ID packet. Table 10–9 shows the descriptions of the various power classes. The default power-class value is loaded following a system (hardware) reset, but is overridden by any value subsequently loaded into the Pwr_Class field in register 4.

Table 10–9. Power Class Descriptions

PC0–PC2	DESCRIPTION
000	Node does not need power and does not repeat power.
001	Node is self-powered and provides a minimum of 15 W to the bus.
010	Node is self-powered and provides a minimum of 30 W to the bus.
011	Node is self-powered and provides a minimum of 45 W to the bus.
100	Node may be powered from the bus and is using up to 3 W. No additional power is needed to enable the link.
101	Reserved
110	Node is powered from the bus and uses up to 3 W. An additional 3 W is needed to enable the link.
111	Node is powered from the bus and uses up to 3 W. An additional 7 W is needed to enable the link.

Not Recommended for New Designs

11 Electrical Characteristics

11.1 Absolute Maximum Ratings Over Operating Temperature Ranges †

Supply voltage range:	V_{DD_33}	–0.5 V to 3.6 V
	V_{DD_15}	–0.5 V to 1.65 V
Input voltage range,	V_I: PCI Express (RX)	–0.6 V to 0.6 V
	V_I: PCI Express REFCLK (single-ended)	–0.5 V to V_{DD_33} + 0.5 V
	V_I: PCI Express REFCLK (differential)	–0.5 V toV_{DD_15} + 0.5 V
	V_I: Miscellaneous 3.3-V IO	–0.5 V to V_{DD_33} + 0.5 V
	V_I: 1394a PHY	–0.5 V to V_{DD_33} + 0.5 V
Output voltage range:	V_O: PCI Express (TX)	–0.5 V to V_{DD_15} + 0.5V
	V_O: Miscellaneous 3.3-V IO	–0.5 V to V_{DD_33} + 0.5 V
	V_O: 1394a PHY	–0.5 V to V_{DD_33} + 0.5 V
Input clamp current, (V_I < 0 or V_I > V_{DD}) (see Note 1)		±20 mA
Output clamp current, (V_O < 0 or V_O > V_{DD}) (see Note 2)		±20 mA
Human body model (HBM) ESD performance		1500 V
Charged device model (CDM) ESD performance		500 V
Storage temperature range, T_{stg}		–65°C to 150°C

† Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Applies for external input and bidirectional buffers. V_I < 0 or V_I > V_{DD} or V_I > V_{CCP}.
2. Applies to external output and bidirectional buffers. V_O < 0 or V_O > V_{DD} or V_O > V_{CCP}.

11.2 Recommended Operation Conditions

		OPERATION	MIN	NOM	MAX	UNITS
V_{DD_15}	Supply voltage	1.5 V	1.35	1.5	1.65	V
V_{DDA_15}						
V_{DD_33}	Supply voltage (I/O)	3.3 V	3	3.3	3.6	V
V_{DDA_33}						
$V_{DDA_33_AUX}$						
T_A	Operating ambient temperature range		0	25	70	°C
T_J	Virtual junction temperature (Note 3)		0	25	115	°C

NOTE 3: The junction temperature reflects simulated conditions. The customer is responsible for verifying junction temperature.

Not Recommended for New Designs

11.3 PCI Express Differential Transmitter Output Ranges

PARAMETER	TERMINALS	MIN	NOM	MAX	UNITS	COMMENTS
UI Unit interval	TXP, TXN	399.88	400	400.12	ps	Each UI is 400 ps ±300 ppm. UI does not account for SSC dictated variations. See Note 4.
$V_{TX\text{-}DIFFp\text{-}p}$ Differential peak-to-peak output voltage	TXP, TXN	0.8		1.2	V	$V_{TX\text{-}DIFFp\text{-}p} = 2*\lvert V_{TXP} - V_{TXN}\rvert$ See Note 5.
$V_{TX\text{-}DE\text{-}RATIO}$ De-emphasized differential output voltage (ratio)	TXP, TXN	–3.0	–3.5	–4.0	dB	This is the ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition. See Note 5.
$T_{TX\text{-}EYE}$ Minimum TX eye width	TXP, TXN	0.75			UI	The maximum transmitter jitter can be derived as $T_{TXMAX\text{-}JITTER} = 1 - T_{TX\text{-}EYE} = 0.3$ UI See Notes 5 and 6.
$T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ Maximum time between the jitter median and maximum deviation from the median	TXP, TXN			0.15	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX\text{-}DIFFp\text{-}p} = 0$ V) in relation to recovered TX UI. A recovered TX UI is calculated over 3500 consecutive UIs of sample data. Jitter is measured using all edges of the 250 consecutive UIs in the center of the 3500 UIs used for calculating the TX UI. See Notes 5 and 6.
$T_{TX\text{-}RISE}$, $T_{TX\text{-}FALL}$ P/N TX output rise/fall time	TXP, TXN	0.125			UI	See Notes 5 and 8.
$V_{TX\text{-}CM\text{-}ACp}$ RMS ac peak common mode output voltage	TXP, TXN			20	mV	$V_{TX\text{-}CM\text{-}ACp} = RMS(\lvert V_{TXP} + V_{TXN}\rvert/2 - V_{TX\text{-}CM\text{-}DC})$ $V_{TX\text{-}CM\text{-}DC} = DC_{(avg)}$ of $\lvert V_{TXP} + V_{TXN}\rvert/2$ See Note 5.
$V_{TX\text{-}CM\text{-}DC\text{-}ACTIVE\text{-}IDLE\text{-}DELTA}$ Absolute delta of dc common mode voltage during L0 and electrical idle.	TXP, TXN	0		100	mV	$\lvert V_{TX\text{-}CM\text{-}DC} - V_{TX\text{-}CM\text{-}Idle\text{-}DC}\rvert \le 100$ mV $V_{TX\text{-}CM\text{-}DC} = DC_{(avg)}$ of $\lvert V_{TXP} + V_{TXN}\rvert/2$ [during L0] $V_{TX\text{-}CM\text{-}Idle\text{-}DC} = DC_{(avg)}$ of $\lvert V_{TXP} + V_{TXN}\rvert/2$ [during electrical idle] See Note 5.
$V_{TX\text{-}CM\text{-}DC\text{-}LINE\text{-}DELTA}$ Absolute delta of dc common mode voltage between P and N	TXP, TXN	0		25	mV	$\lvert V_{TXP\text{-}CM\text{-}DC} - V_{TXN\text{-}CM\text{-}DC}\rvert \le 25$ mV when $V_{TXP\text{-}CM\text{-}DC} = DC_{(avg)}$ of $\lvert V_{TXP}\rvert$ $V_{TXN\text{-}CM\text{-}DC} = DC_{(avg)}$ of $\lvert V_{TXN}\rvert$ See Note 5.
$V_{TX\text{-}IDLE\text{-}DIFFp}$ Electrical idle differential peak output voltage	TXP, TXN	0		20	mV	$V_{TX\text{-}IDLE\text{-}DIFFp} = \lvert V_{TXP\text{-}Idle} - V_{TXN\text{-}Idle}\rvert \le 20$ mV See Note 5.
$V_{TX\text{-}RCV\text{-}DETECT}$ The amount of voltage change allowed during receiver detection	TXP, TXN			600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance receiver is present.
$V_{TX\text{-}DC\text{-}CM}$ The TX dc common mode voltage	TXP, TXN	0		3.6	V	The allowed dc common mode voltage under any condition.

PCI Express Differential Transmitter Output Ranges (continued)

PARAMETER	TERMINALS	MIN	NOM	MAX	UNITS	COMMENTS
$I_{TX\text{-}SHORT}$ TX short circuit current limit	TXP, TXN			90	mA	The total current the transmitter can provide when shorted to its ground.
$T_{TX\text{-}IDLE\text{-}MIN}$ Minimum time spent in electrical idle	TXP, TXN	50			UI	Minimum time a transmitter must be in electrical Idle. Utilized by the receiver to start looking for an electrical idle exit after successfully receiving an electrical idle ordered set.
$T_{TX\text{-}IDLE\text{-}SET\text{-}to\text{-}IDLE}$ Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set	TXP, TXN			20	UI	After sending an electrical idle ordered set, the transmitter must meet all electrical idle specifications within this time. This is considered a debounce time for the transmitter to meet electrical idle after transitioning from L0.
$T_{TX\text{-}IDLE\text{-}to\text{-}DIFF\text{-}DATA}$ Maximum time to transition to valid TX specifications after leaving an electrical idle condition	TXP, TXN			20	UI	Maximum time to meet all TX specifications when transitioning from electrical idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving electrical idle.
$RL_{TX\text{-}DIFF}$ Differential return loss	TXP, TXN	10			dB	Measured over 50 MHz to 1.25 GHz. See Note 7.
$RL_{TX\text{-}CM}$ Common mode return loss	TXP, TXN	6			dB	Measured over 50 MHz to 1.25 GHz. See Note 7.
$Z_{TX\text{-}DIFF\text{-}DC}$ DC differential TX impedance	TXP, TXN	80	100	120	Ω	TX dc differential mode low impedance
$Z_{TX\text{-}DC}$ Transmitter dc impedance	TXP, TXN	40			Ω	Required TXP as well as TXN dc impedance during all states
C_{TX} AC coupling capacitor	TXP, TXN	75		200	nF	All transmitters are ac-coupled and are required on the PWB.

NOTES:
4. No test load is necessarily associated with this value.
5. Specified at the measurement point into a timing and voltage compliance test load and measured over any 250 consecutive TX UIs.
6. A $T_{TX\text{-}EYE}$ = 0.75 UI provides for a total sum of deterministic and random jitter budget of $T_{TX\text{-}JITTER\text{-}MAX}$ = 0.25 UI for the transmitter collected over any 250 consecutive TX UIs. The $T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
7. The transmitter input impedance results in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 Ω to ground for both the P and N lines. Note that the series capacitors C_{TX} is optional for the return loss measurement.
8. Measured between 20% and 80% at transmitter package terminals into a test load for both V_{TXP} and V_{TXN}.

11.4 PCI Express Differential Receiver Input Ranges

PARAMETER	TERMINALS	MIN	NOM	MAX	UNITS	COMMENTS
UI Unit interval	RXP, RXN	399.88	400	400.12	ps	Each UI is 400 ps ±300 ppm. UI does not account for SSC dictated variations. See Note 9.
$V_{RX\text{-}DIFFp\text{-}p}$ Differential input peak-to-peak voltage	RXP, RXN	0.175		1.200	V	$V_{RX\text{-}DIFFp\text{-}p} = 2*\lvert V_{RXP} - V_{RXN}\rvert$ See Note 10.
$T_{RX\text{-}EYE}$ Minimum receiver eye width	RXP, RXN	0.4			UI	The maximum interconnect media and transmitter jitter that can be tolerated by the receiver is derived as $T_{RX\text{-}MAX\text{-}JITTER} = 1 - T_{RX\text{-}EYE} = 0.6$ UI See Notes 10 and 11.
$T_{RX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ Maximum time between the jitter median and maximum deviation from the median	RXP, RXN			0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX\text{-}DIFFp\text{-}p} = 0$ V) in relation to recovered TX UI. A recovered TX UI is calculated over 3500 consecutive UIs of sample data. Jitter is measured using all edges of the 250 consecutive UIs in the center of the 3500 UIs used for calculating the TX UI. See Notes 10 and 11.
$V_{RX\text{-}CM\text{-}ACp}$ AC peak common mode input voltage	RXP, RXN			150	mV	$V_{RX\text{-}CM\text{-}ACp} = RMS(\lvert V_{RXP} + V_{RXN}\rvert/2 - V_{RX\text{-}CM\text{-}DC})$ $V_{RX\text{-}CM\text{-}DC} = DC_{(avg)}$ of $\lvert V_{RXP} + V_{RXN}\rvert/2$ See Note 10.
$RL_{RX\text{-}DIFF}$ Differential return loss	RXP, RXN	10			dB	Measured over 50 MHz to 1.25 GHz with the P and N lines biased at +300 mV and –300 mV, respectively. See Note 12.
$RL_{RX\text{-}CM}$ Common mode return loss	RXP, RXN	6			dB	Measured over 50 MHz to 1.25 GHz with the P and N lines biased at +300 mV and –300 mV, respectively. See Note 12.
$Z_{RX\text{-}DIFF\text{-}DC}$ DC differential input impedance	RXP, RXN	80	100	120	Ω	RX dc differential mode impedance See Note 13.
$Z_{RX\text{-}DC}$ DC input impedance	RXP, RXN	40	50	60	Ω	Required RXP as well as RXN dc impedance (50 Ω ±20% tolerance). See Notes 10 and 13.
$Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC}$ Powered down dc input impedance	RXP, RXN	200k			Ω	Required RXP as well as RXN dc impedance when the receiver terminations do not have power. See Note 14.
$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p}$ Electrical idle detect threshold	RXP, RXN	65		175	mV	$V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p} = 2*\lvert V_{RXP} - V_{RXN}\rvert$ measured at the receiver package terminals
$T_{RX\text{-}IDLE\text{-}DET\text{-}DIFF\text{-}ENTER\text{-}TIME}$ Unexpected electrical idle enter detect threshold integration time	RXP, RXN			10	ms	An unexpected electrical idle ($V_{RX\text{-}DIFFp\text{-}p} < V_{RX\text{-}IDLE\text{-}DET\text{-}DIFFp\text{-}p}$) must be recognized no longer than $T_{RX\text{-}IDLE\text{-}DET\text{-}DIFF\text{-}ENTER\text{-}TIME}$ to signal an unexpected idle condition.

NOTES: 9. No test load is necessarily associated with this value.
10. Specified at the measurement point and measured over any 250 consecutive UIs. A test load must be used as the RX device when taking measurements. If the clocks to the RX and TX are not derived from the same reference clock, then the TX UI recovered from 3500 consecutive UI is used as a reference for the eye diagram.

11. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total UI jitter budget collected over any 250 consecutive TX UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, then the TX UI recovered from 3500 consecutive UIs must be used as the reference for the eye diagram.
12. The receiver input impedance results in a differential return loss greater than or equal to 15 dB with the P line biased to 300 mV and the N line biased to –300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the P and N line (i.e., as measured by a Vector Network Analyzer with 50-Ω probes). The series capacitors C_{TX} is optional for the return loss measurement.
13. Impedance during all link training status state machine (LTSSM) states. When transitioning from a PCI Express reset to the detect state (the initial state of the LTSSM) there is a 5-ms transition time before receiver termination values must be met on the unconfigured lane of a port.
14. The RX dc common mode impedance that exists when no power is present or PCI Express reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.

11.5 PCI Express Differential Reference Clock Input Ranges

PARAMETER	TERMINALS	MIN	NOM	MAX	UNITS	COMMENTS
$f_{IN-DIFF}$ Differential input frequency	REFCLK+ REFCLK–		100		MHz	The input frequency is 100 MHz + 300 ppm and – 2800 ppm including SSC-dictated variations.
f_{IN-SE} Single-ended input frequency	REFCLK+		125		MHz	The input frequency is 125 MHz + 300 ppm and – 300 ppm.
$V_{RX-DIFFp-p}$ Differential input peak-to-peak voltage	REFCLK+ REFCLK–	0.175		1.200	V	$V_{RX-DIFFp-p} = 2*\|V_{REFCLK+} - V_{REFCLK-}\|$
V_{IH-SE}	REFCLK+	0.7 V_{DD_33}		V_{DD_33}	V	Single-ended, reference clock mode high-level input voltage
V_{IL-SE}	REFCLK+	0		0.3 V_{DD_33}	V	Single-ended, reference clock mode low-level input voltage
$V_{RX-CM-ACp}$ AC peak common mode input voltage	REFCLK+ REFCLK–			140	mV	$V_{RX-CM-ACp} = RMS(\|V_{REFCLK+} + V_{REFCLK-}\|/2 - V_{RX-CM-DC})$ $V_{RX-CM-DC} = DC_{(avg)}$ of $\|V_{REFCLK+} + V_{REFCLK-}\|/2$
Duty cycle	REFCLK+ REFCLK–	40%		60%		Differential and single-ended waveform input duty cycle
$Z_{RX-DIFF-DC}$ DC differential input impedance	REFCLK+ REFCLK–		20		kΩ	REFCLK+/– dc differential mode impedance
Z_{RX-DC} DC input impedance	REFCLK+ REFCLK–		20		kΩ	REFCLK+ dc single-ended mode impedance

NOTE 15: The XIO2200A is compliant with the defined system jitter models for a PCI-Express reference clock and associated TX/RX link. These system jitter models are described in the *PCI-Express Jitter Modeling*, Revision 1.0RD document. Any usage of the XIO2200A in a system configuration that does not conform to the defined system jitter models requires the system designer to validate the system jitter budgets.

11.6 Electrical Characteristics Over Recommended Operating Conditions (3.3-V I/O)

PARAMETER		OPERATION	TEST CONDITIONS	MIN	MAX	UNITS
V_{IH}	High-level input voltage (Note 16)	V_{DD_33}		0.7 V_{DD_33}	V_{DD_33}	V
V_{IL}	Low-level input voltage (Note 16)	V_{DD_33}		0	0.3 V_{DD_33}	V
V_I	Input voltage			0	V_{DD_33}	V
V_O	Output voltage (Note 17)			0	V_{DD_33}	V
t_T	Input transition time (t_{rise} and t_{fall})			0	25	ns
V_{hys}	Input hysteresis (Note 18)				0.13 V_{DD_33}	V
V_{OH}	High-level output voltage	V_{DD_33}	I_{OH} = –4 mA	0.8 V_{DD_33}		V
V_{OL}	Low-level output voltage	V_{DD_33}	I_{OL} = 4 mA		0.22 V_{DD_33}	V
I_{OZ}	High-impedance, output current (Note 17)	V_{DD_33}	V_I = 0 to V_{DD_33}		±20	µA
I_{OZP}	High-impedance, output current with internal pullup or pulldown resistor (Note 19)	V_{DD_33}	V_I = 0 to V_{DD_33}		±100	µA
I_I	Input current (Note 20)	V_{DD_33}	V_I = 0 to V_{DD_33}		±1	µA

NOTES: 16. Applies to external inputs and bidirectional buffers.
17. Applies to external outputs and bidirectional buffers.
18. Applies to $\overline{PERST}$ and $\overline{GRST}$.
19. Applies to $\overline{GRST}$ (pullup resistor) and most GPIO (pullup resistor).
20. Applies to external input buffers.

NOTE: This table applies to $\overline{PERST}$, $\overline{WAKE}$, REFCLK_SEL, $\overline{GRST}$, GPIO7:0, CNA, PC2:0, and all RSVD terminals.

11.7 Electrical Characteristics Over Recommended Operating Conditions (1394a PHY Port Driver)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNITS
V_{OD}	Differential output voltage	56 Ω, see Figure 11–1	172	265	mV
I_{DIFF}	Driver difference current. TPA+, TPA–, TPB+, TPB–	Drivers enabled, speed signaling off	–1.05†	1.05†	mA
I_{SP200}	Common-mode speed signaling current. TPB+, TPB–	S200 speed signaling enabled	–4.84‡	–2.53‡	mA
I_{SP400}	Common-mode speed signaling current. TPB+, TPB–	S400 speed signaling enabled	–12.4‡	–8.1‡	mA
V_{OFF}	Off state differential voltage	Drivers disabled		20	mV

† Limits defined as algebraic sum of TPA+ and TPA– driver currents. Limits also apply to algebraic sum of TPB+ and TPB– driver currents.
‡ Limits defined as absolute limit of each of TPB+ and TPB– driver currents.

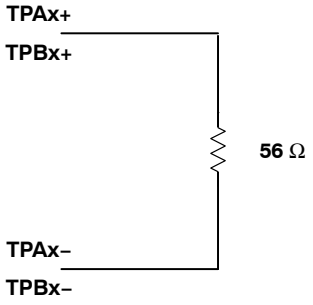

Figure 11–1. Test Load Diagram

11.8 Thermal Information

THERMAL METRIC†		XIO2200A ZGW (176 PINS)	UNITS
θ_{JA}	Junction–to–ambient thermal resistance	39.2	°C/W
θ_{JCtop}	Junction–to–ambient (top) thermal resistance	8.9	
θ_{JB}	Junction–to–board thermal resistance	20.1	
Ψ_{JT}	Junction–to–top charactaerization parameter	0.3	
Ψ_{JB}	Junction–to–board characterization parameter	20.4	
θ_{JCbot}	Junction–to–case (bottom) thermal resistance	N/A	

† For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

11.9 Switching Characteristics for 1394a PHY Port Driver

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
	Jitter, transmit	Between TPA and TPB			±0.15	ns
	Skew, transmit	Between TPA and TPB			±0.1	ns
t_r	TP differential rise time, transmit	10% to 90%, at 1394 connector	0.5		1.2	ns
t_f	TP differential fall time, transmit	90% to 10%, at 1394 connector	0.5		1.2	ns

11.10 Electrical Characteristics Over Recommended Operating Conditions (1394a PHY Port Receiver)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
Z_{ID}	Differential impedance	Drivers disabled	4	7		kΩ
					4	pF
Z_{IC}	Common-mode impedance	Drivers disabled	20			kΩ
					24	pF
V_{TH-R}	Receiver input threshold voltage	Drivers disabled	–30		30	mV
V_{TH-CB}	Cable bias detect threshold. TPBx cable inputs	Drivers disabled	0.6		1	V
V_{TH+}	Positive arbitration comparator threshold voltage	Drivers disabled	89		168	mV
V_{TH-}	Negative arbitration comparator threshold voltage	Drivers disabled	–168		–89	mV
$V_{TH-SP200}$	Speed signal threshold	TPBIAS–TPA common mode voltage, drivers disabled	49		131	mV
$V_{TH-SP400}$	Speed signal threshold	TPBIAS–TPA common mode voltage, drivers disabled	314		396	mV
V_{ID}	Differential input voltage	Cable inputs, during data reception	118		260	mV
		Cable inputs, during arbitration	168		265	
V_{IC}	Common-mode input voltage	TPB cable inputs, source power node	0.4706		2.515	V
		TPB cable inputs, nonsource power node†	0.4706		2.015	

† For a node that does not source power, see IEEE Std 1394a-2000.

Not Recommended for New Designs

11.11 Jitter/Skew Characteristics for 1394a PHY Port Receiver

PARAMETER		MIN	TYP	MAX	UNITS
Receive input jitter	TPA, TPB cable inputs, S100 operation			±1.08	ns
	TPA, TPB cable inputs, S200 operation			±0.5	ns
	TPA, TPB cable inputs, S400 operation			±0.315	ns
Receive input skew	Between TPA and TPB cable inputs, S100 operation			±0.8	ns
	Between TPA and TPB cable inputs, S200 operation			±0.55	ns
	Between TPA and TPB cable inputs, S400 operation			±0.5	ns

11.12 Operating, Timing, and Switching Characteristics of XI

PARAMETER		MIN	TYP	MAX	UNITS
V_{IH}	High-level input voltage	0.63 V_{DDA_33}			V
V_{IL}	Low-level input voltage			0.33 V_{DDA_33}	V
	Input clock frequency		24.576		MHz
	Input clock frequency tolerance			<100	ppm
	Input slew rate	0.2		4	V/ns
	Input clock duty cycle	40%		60%	

11.13 Electrical Characteristics Over Recommended Operating Conditions (1394a Miscellaneous I/O)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{TH}	Power status threshold CPS input †	400-kΩ resistor †	4.7		7.5	V
V_O	TPBIAS output voltage	At rated I_O current	1.665		2.015	V
I_O	TPBIAS output current		−5.6		1.3	mA

† Measure at cable power side of resistor.

Not Recommended for New Designs

12 Glossary

ACRONYM	DEFINITION
BIST	Built-in self test
ECRC	End-to-end cyclic redundancy code
EEPROM	Electrically erasable programmable read-only memory
GP	General purpose
GPIO	General-purpose input output
ID	Identification
IF	Interface
IO	Input output
I2S	Inter IC sound
LPM	Link power management
LSB	Least significant bit
MSB	Most significant bit
MSI	Message signaled interrupts
PCI	Peripheral component interface
PME	PCI power management event
QoS	Quality-of-service
RX	Receive
SCL	Serial-bus clock
SDA	Serial-bus data
TC	Traffic class
TLP	Transaction layer packet or protocol
TX	Transmit
VC	Virtual channel
WRR	Weighted round-robin

Not Recommended for New Designs

13 Mechanical Data

The XIO2200A device is available in the 175−ball lead−free (Pb atomic number 82) MicroStar BGA package (ZHH), the 176-ball MicroStar BGA package (GGW), or the 176-ball lead-free (Pb atomic number 82) MicroStar BGA package (ZGW). The following figures show the mechanical dimensions for the packages. The GGW and ZGW packages are mechanically identical.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XIO2200AZGW	LIFEBUY	BGA MICROSTAR	ZGW	176	126	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR		XIO2200A	
XIO2200AZHH	LIFEBUY	BGA MICROSTAR	ZHH	175	160	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR		XIO2200A	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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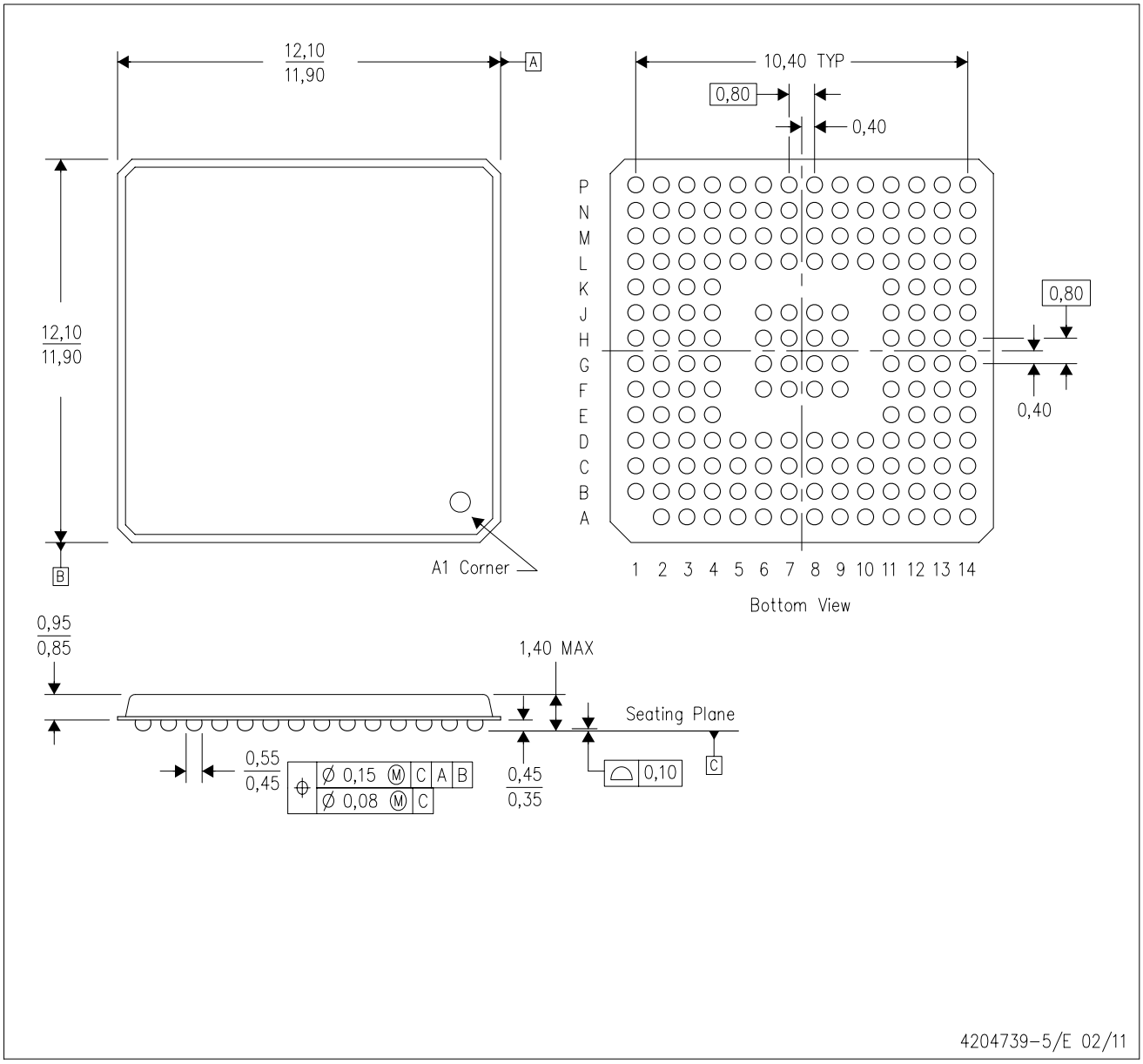
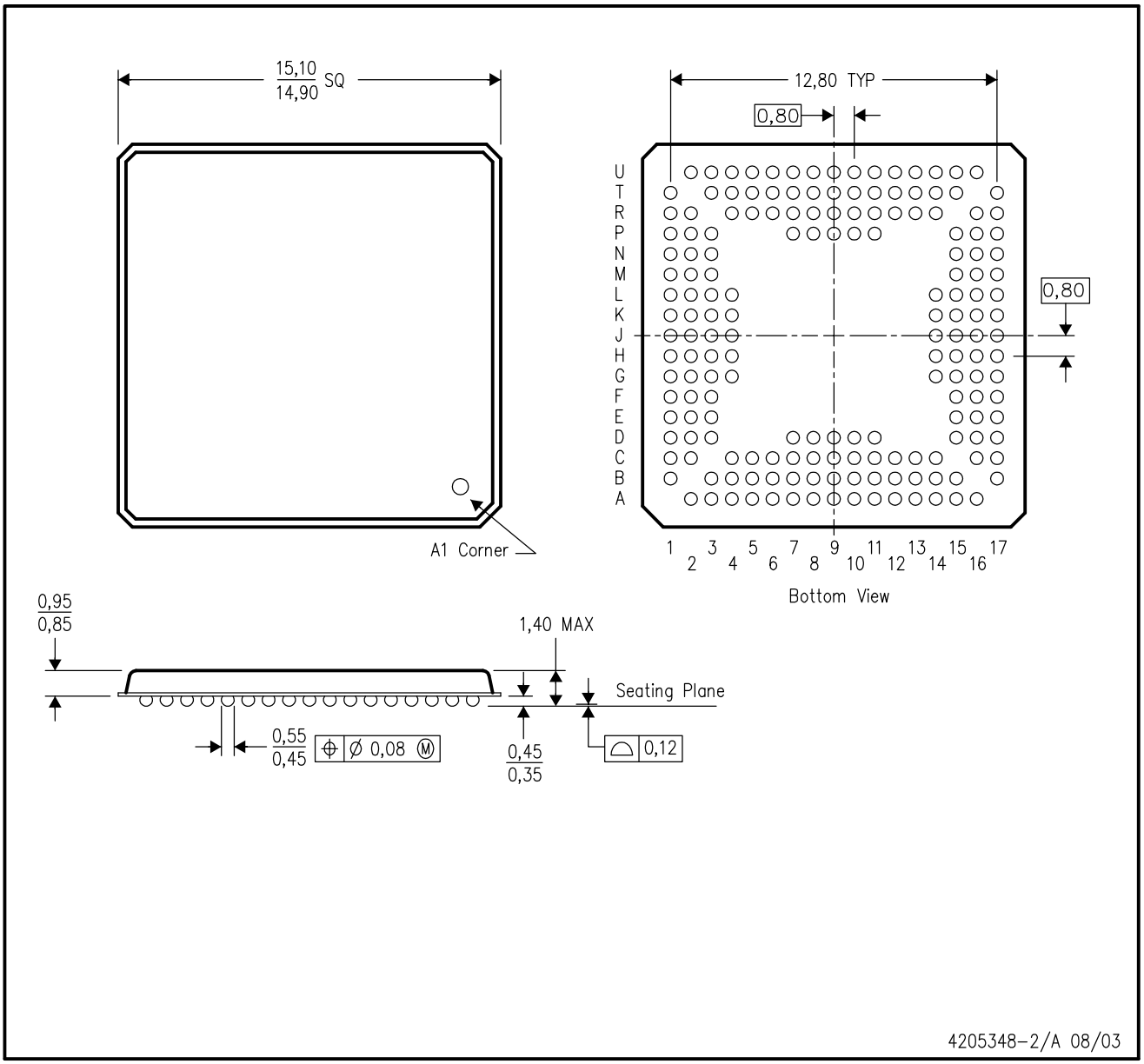
ZHH (S–PBGA–N175) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar BGA configuration.
D. This is a Pb–free solder ball design.

MicroStar is a trademark of Texas Instruments.

ZGW (S–PBGA–N176) PLASTIC BALL GRID ARRAY



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. MicroStar BGA™ configuration
- D. This package is lead–free.

MicroStar BGA is a trademark of Texas Instruments.

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